Wafer-level Backside Process Technology for Forming High-density Vias and Backside Metal Patterning for 50-μm-thick InP Substrate

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Abstract

   A wafer-level backside process for an InP substrate is developed for stable operation of InP-based sub-millimeter-wave monolithic ICs. The developed backside process consists of thinning a 3-inch InP substrate down to 50 μm, forming dense vias, and patterning backside metal, and dicing the 50-μm-thick InP substrate. Vias can be formed with a narrow edge-to-edge gap of 35 μm and a small deviation of 1.8 % across the whole 50-μm-thick substrate. We also successfully demonstrate backside metal patterning with good alignment accuracy of better than 1 μm for the devices formed on the topside and crack-free dicing of the fragile 50-μm-thick InP substrate.

INTRODUCTION

   Recently, InP-based sub-millimeter-wave monolithic ICs (SMMICs) have attracted much attention because they are key components in broadband wireless communications systems[1] and terahertz imaging systems[2]. For stable operation of SMMICs, a wafer-level backside process for thinning down a substrate and forming ground vias is necessary in order to eliminate ground bounce and substrate resonance. Some successful demonstrations of SMMICs owing to a thinned substrate and incorporated ground vias have been presented [3, 4]. However, details about the technologies for thinning down the substrate and forming backside ground vias have not been reported despite of their importance. Though a thinner substrate and denser ground vias is more effective for stable operation of SMMICs, these technologies become more difficult. Thus, the structural requirements, such as the substrate thickness and the size and spacing of vias, should be clarified and then the backside process should be developed on the basis of those requirements in order to avoid the irrelative difficulty.

   Here, we present wafer-level backside process technologies consisting of thinning a 3-inch InP substrate, forming dense vias, patterning backside metals, and dicing the InP substrate. The process is developed considering the structural requirements about target substrate thickness and the size and spacing of vias derived from simple calculations, so as to ensure proper operation of SMMICs. We also

discuss the uniformity of the fabricated vias and the necessity of scaling them down.

PROCESS TECHNOLOGY

   First, we clarified the required thickness InP substrate thickness, via size and spacing. The RF transmission properties of the thinned substrate with vias were evaluated up to 1 THz with a simple model where the fundamental mode propagates from one end-face of the chip to the other. As shown in Fig. 1, distractive transmission, which causes substrate resonance, can be eliminated with IC stability maintained up to Y-band operation when the chip is thinned down to 50 μm and the vias are formed with a diameter of 50 μm and an edge-to-edge gap of 50 μm. In contrast, some distractive transmissions at frequencies ranging up to 500
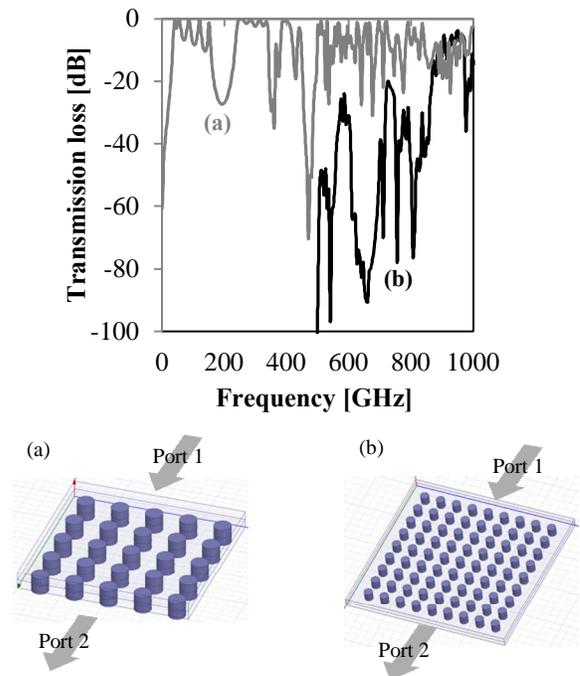

Fig. 1. Simulated RF transmission of the thinned substrate with vias. (a) A 100-μm-thick substrate and 100-μm-gap vias. (b) A 50-μm-thick substrate and 50-μm-gap vias.

GHz are observed when the chip is thinned down only to 100 μm and vias are formed with a relatively large diameter of 100 μm and a relatively wide edge-to-edge gap of 100 μm. Thus, our backside process was developed to achieve the above.

The backside process begins with thinning down a 3-inch InP substrate after topside IC formation. This is followed by etching the substrate to form vias, electroplating, metal-patterning, and dicing the substrate. Throughout the process, the thin fragile InP substrate is adhered upside down to a glass substrate (Fig. 2).
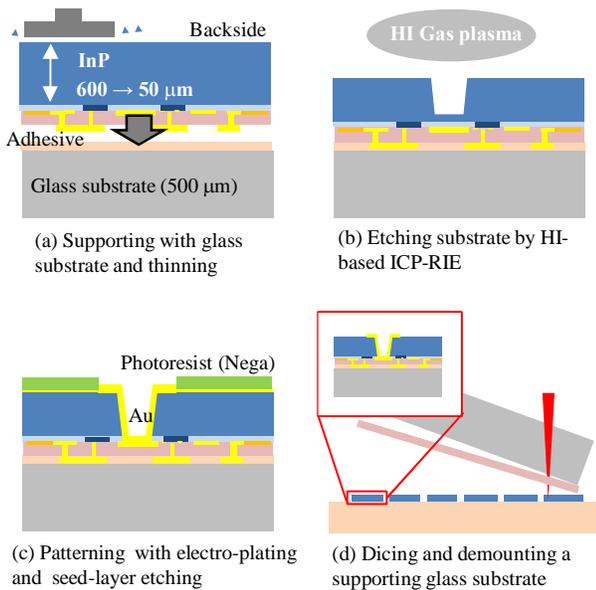

(a) Supporting with glass substrate and thinning

(b) Etching substrate by HI-based ICP-RIE

(c) Patterning with electro-plating and seed-layer etching

(d) Dicing and demounting a supporting glass substrate

Fig. 2. Developed wafer-level backside process.

An InP substrate with an original thickness of 600 μm is supported on the 500-μm-thick glass substrate with UV-cured adhesive after IC formation and ground down to 50 μm. To ensure uniform thinning, the InP substrate should be supported parallel to the glass substrate. In our process, the parallelism between the InP and glass substrate is kept at better than 2 μm, which is fine enough to guarantee uniform thinning.

Next, inductively coupled plasma reactive ion etching (ICP-RIE) with HI as etching gas is performed to make vias. Polybenzoxazole (PBO) is selected as an etching mask because of its high etching selectivity to InP of 16 and high heat durability at temperatures over 250 ^{o}C. The higher etching selectivity is preferable in order to avoid widening of the via diameter from the designed one and increasing the mask thickness, which causes difficulty in mask patterning. The high heat durability is necessary in order to keep room for optimizing the etching condition. Here, a SiO_2 film is deposited on the InP substrate to ensure the adherence of the

PBO. Good adherence contributes to the controllability of the shape of the vias by suppressing side-etching during the ICP-RIE caused by unintentional random detachment of the etching mask. As the halogenated production of the etched InP efficiently sublimates at over 150 ^{o}C[5], we can obtain finely shaped vias without residue by keeping the substrate temperature higher than 150 ^{o}C during the ICP-RIE. However, this lower limit is not the only requirement for the substrate temperature because the InP etching rate is very sensitive to temperature, especially higher than 150 ^{o}C. If the temperature is not both uniform across the 3-inch substrate and constant during the etching, the geometries of the formed vias show significant deviation over the whole substrate and in every run. Furthermore, the temperature should be lower than the temperature limit (172 ^{o}C) of the adhesive layer degradation. To satisfy this tight limitation, we achieve precise and reproducible control of the substrate temperature by introducing an intermittent cooling step between the etching steps. In this way, we can avoid an increase and fluctuation in the substrate temperature due to the long-time and non-uniform plasma exposure. We obtained an InP etching rate of about 1.5 μm/minute with good reproducibility and stability in every run, and with good uniformity across the substrate. With the developed etching sequence, we successfully fabricated the vias without residue, and with good shape uniformity and size controllability as shown in Fig. 3.
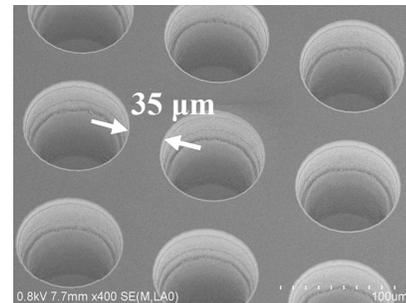

Fig. 3. SEM image of fabricated 80-μm-diameter vias with an edge-to-edge gap of 35 μm.

Then, we performed the metallization of the backside of the substrate and the inside of the vias, and the metal patterning. A simple way to form ground vias is just to metalize the inside of vias and the whole area of the backside. However, the metal for the ground should be partly removed, especially that on dicing lines because it causes cracks or defects in the InP substrate when the substrate is diced. In addition, some chips require backside metal patterning in order to ensure their circuit performance. For an on-chip antenna for sub-millimeter-wave applications, the backside metal beneath the antenna pattern must be removed in order to properly receive the sub-millimeter-wave signal. Thus, the metal patterning is essential. The backside ground metal is formed as follows. After the Au seed layer is sputtered on the backside of the substrate and

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the inside of the vias, selective electroplating is performed with a spray-coated nega-type resist mask. The use of the nega-type resist avoids under-exposed resist residue inside the vias, which could be a critical issue at resist development when posi-type resist is used. The spray coating ensures conformal resist coverage on the bottom and the inside wall of the 50-μm-deep vias. The resist is patterned by a reverse-side alignment technique with a contact aligner. After selective electroplating, the Au seed layer is removed by conventional RIE, and we finally have a chip with ground vias formed and the backside patterned. Figure 4 shows a cross-sectional SEM image of a fabricated Au-electroplated via. A 7-μm-thick electroplated Au layer conformally covers the inside wall of the via without voids or defects, and the bottom of the via is covered with uniform 4-μm-thick electroplated Au, which is connected with the topside metal layer. Figure 5 shows SEM images of (a) the patterned backside metal with densely formed vias, and (b) an on-chip antenna with the ground vias and the patterned ground metal. Here, alignment accuracy between the topside and backside pattern is better than 1 μm.
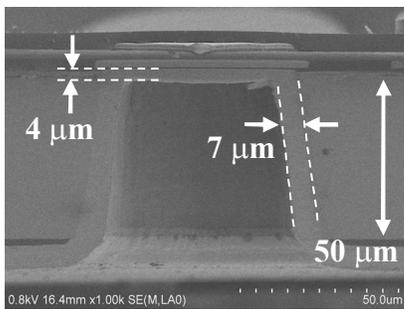
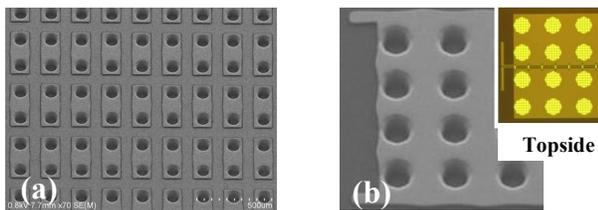Fig. 4. Cross-sectional SEM image of Au-electroplated via.

Fig. 5. SEM images of (a) patterned backside metal with densely formed vias, and (b) a backside-patterned on-chip antenna.

Finally, the backside-patterned InP substrate is diced into a chip from the backside. In a conventional technique, a substrate is transferred to an adhesive rubber film prior to its dicing. However, this technique is not applicable to a free-standing 50-μm thinned and via-formed InP substrate because the substrate is very fragile and easily broken by physical damage, such as oscillation during dicing or tensile bending when the diced InP chip is peeled from the adhesive rubber film. Supporting the InP substrate with a solid

material is one of the solutions to avoid the physical damage during dicing. Thus, we dice the InP substrate with it supported by the glass substrate. The diced InP chip is then transferred to an adhesive rubber film, followed by removal of the glass substrate by carbonizing the adhesive between the InP and glass substrate with laser irradiation. In this way, we can successfully obtain a crack-free diced InP chip (Fig. 6).
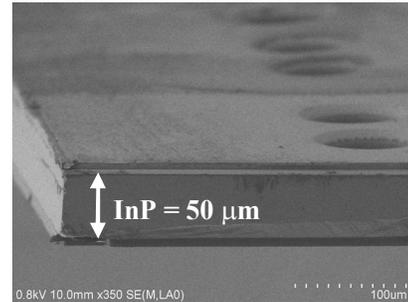
Fig. 6. Cross-sectional SEM image of crack-free diced InP chip.

DISCUSSION

The size of the fabricated vias with various diameters is shown in Fig. 7. The topside diameters are almost same as the designed ones, and the backside ones are larger than the topside ones for each via size. The tapered shapes with the vias broadening toward the backside are preferable for forming a conformal deposition of a metal seed layer for electroplating.

Plotted error bars for each via size show the deviations of the diameter. We obtain uniform geometry of vias with a 20- to 100-μm diameter: Ratio of the diameter deviation to
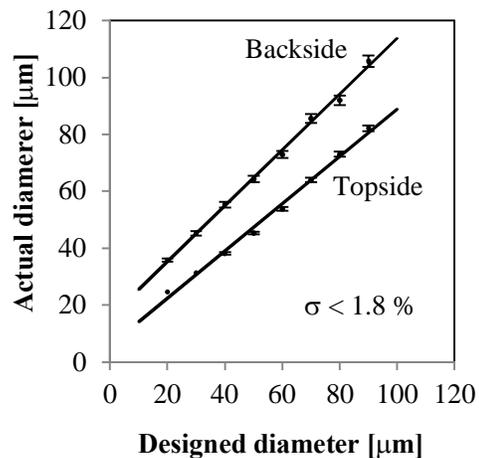
Fig. 7. Actual size of the fabricated vias with a 20- to 100-μm diameter. Error bar indicates the deviation (σ) of the diameter.

the actual diameter (σ_r) is less than 1.8 %. Using the obtained deviations, we can estimate the possible minimum edge-to-edge gap of vias (g_{min}). If the fluctuation of the via diameter is assumed to be 3 σ_r, g_{min} can be simply calculated as $g_{min} = 3\ \sigma_r\ \phi_{bk}$, where ϕ_{bk} denotes the backside diameter of a via. In the case of vias with a 50-μm designed diameter (the actual backside diameter is 64 μm), the estimated g_{min} is about 3.5 μm. This indicates that the obtained uniformity in via shape is good enough to ensure 50-μm edge-to-edge gaps, and points to the possibility of much more dense formation of vias.

The resistivity of vias is very important when we use vias for ground stabilization in ICs because the ground potential on the topside, where the ICs are formed, should be equal to that of the backside ground. We estimated the total resistivity of vias per unit area when the vias are closely formed with the above-mentioned g_{min}. As shown in Fig. 8, with the scaling-down of via diameter, the total resistivity decreases proportionally. This is because of the increase of the total cross-sectional area of the electroplated metal on the bottom of the vias connected to the topside ground layer and the metal on the sidewall of the vias, which act as an interconnection between the topside and backside ground. As σ_r is almost the same for each via size, g_{min} proportionally decreases with via size. Thus, the scaling-down of vias contributes to increasing the number of vias per unit area and results in minimizing total resistivity. Moreover, scaled-down vias are advantageous for improving their layout flexibility in ICs. For instance, small vias can be freely and densely formed in the ICs, leading to more stable ground potential than larger vias are used.

These results suggest that scaling-down of vias and minimizing the gap are significant in ground stabilization, and the fabricated vias exhibiting low resistivity could be applicable to DC or RF interconnection for 3D chip integration.
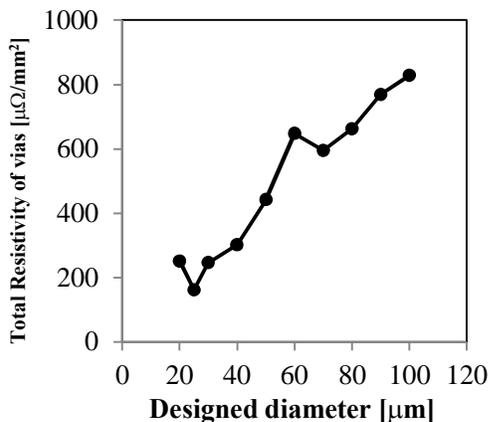

Fig. 8. Dependence of total resistivity of closely formed vias on via diameter.

SUMMARY

We developed wafer-level backside process technology that consists of thinning the substrate down to 50 μm, forming uniform and dense vias, making fine backside metal patterns, and crack-free dicing. The vias are successfully formed with a narrow edge-to-edge gap of 35 μm and a small deviation of 1.8 % across the whole 50-μm-thick substrate by introducing a new etching sequence, which ensures highly reproducible and uniform InP etching. The backside metal patterning with good alignment accuracy of better than 1 μm for devices formed on the topside and the crack-free dicing of the fragile 50-μm-thick InP substrate with a newly developed dicing procedure were also demonstrated. In addition, we clarified the necessity of high-density formation and scaling-down of vias.

The developed wafer-level backside process technology is promising for fabricating SMMIC chips with stable operation and boosting their operating frequency up to 500 GHz.

REFERENCES

[1] C. Jastrow et al., ö300 GHz transmission systemö, Electron. Lett., (2008), Vol. 44, No. 3, pp.213-214.
[2] B. B. Hu et al., öImaging with terahertz wavesö, Opt. Lett., (1995), Vol. 20, No. 16, pp.1716-1718.
[3] W. R. Deal et al., öDemonstration of a 0.48 THz Amplifier Module Using InP HEMT Transistorsö, IEEE Microw. Wireless Compon. Lett., (2010), Vol. 20, No. 5, pp.289-291.
[4] M. Seo et al., öInP HBT IC Technology for Terahertz Frequencies: Fundamental Oscillators Up to 0.57 THzö, IEEE J. Solid-State Circuits, (2011), Vol. 46, No. 10, pp.2203-2214.
[5] R. J. Shul et al., öTemperature Dependent Electron Cyclotron Resonance Etching of InP, GaP, and GaAsö, J. Vac. Sci. Technol. A, Vol. 14, No. 3, pp1102-1106, 1996.