Full-Wafer, Small-Area Via-Hole Fabrication Process Development for Indium-Bearing III-V Heterostructure Devices

Yuning Zhao, Patrick Fay [a]
Department of Electrical Engineering, University of Notre Dame, 275 Fitzpatrick Hall, Notre Dame, IN 46556
a) Tel: (574) 631-5693, Email: pfay@nd.edu

Andree Wibowo, Chris Youtsey
MicroLink Devices, Inc., 6457 W. Howard St., Niles, IL 60714

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Abstract

Three different dry etch chemistries (Cl_2/Ar, BCl_3/Cl_2/Ar, and $SiCl_4$/Ar) were evaluated for full-wafer, small-area via-hole fabrication in indium-bearing III-V heterostructure devices. The process was developed and demonstrated using InGaP/GaAs/InGaAs inverted metamorphic triple-junction backside contact photovoltaic cells as the baseline heterostructure. Uniform, vertical and smooth etch profiles were obtained through the heterostructures, despite the widely varying material compositions. Optical emission spectroscopy was used to track the process in real time for improved process control. The results obtained by etching small test samples are compared with those from full 4" wafers, and the differences in etch behavior are discussed.

INTRODUCTION

A comparison of several process alternatives for forming small-area, high-density vias in Indium-bearing III-V materials by dry etching is presented. While through-wafer via etches are well-established in production, as MMIC operational frequencies increase there is an increasing need for high-density, small-area vias for grounding active devices and suppressing substrate modes. In addition, less conventional devices such as InGaP/GaAs/InGaAs inverted metamorphic multijunction (IMM) triple-junction backside contact photovoltaic cells can also benefit from the ability to form small-area vias in dense arrays [1]. For all of these applications, strongly anisotropic etch profiles are necessary to minimize via area (see Fig. 1 for an example of vias as applied to a backside contact photovoltaic cell). To serve these needs, a study of three different dry etch chemistries (Cl_2/Ar, BCl_3/Cl_2/Ar, and $SiCl_4$/Ar) is reported, and a process based on $SiCl_4$/Ar that results in very smooth sidewalls with good etch profiles has been identified.

EXPERIMENTAL APPROACH

For the process development shown here, vias were formed in triple-junction solar cell epitaxial material (see Fig. 1 for details). This places extreme demands on the via fabrication process, since straight sidewalls through materials with widely varying composition (especially In content) is challenging. The processes shown here can be translated to the simpler case of single-material vias with minor tuning. The process development was carried out in an Oerlikon Shuttleline inductively coupled plasma reactive ion etching (ICP-RIE) system with helium backside cooling. An SiO_2 layer grown by plasma-enhanced chemical vapor deposition (PECVD) was used as the hard mask. To provide improved process monitoring and robustness, optical emission spectroscopy (OES) was used to monitor the etch progress in real time. In addition, an exploration of the validity of doing process development on small test samples (of dimensions 0.5 cm x 0.5 cm) vs. development on full 4" wafers was performed. For the study of etching using small test samples, vacuum-compatible thermal grease was used to improve the thermal contact between the small samples and the 4" carrier wafer, and the impact of the carrier wafer composition was evaluated for several different carrier wafer types, including bare Si and Si wafers coated with either PECVD SiN_x or SiO_2.

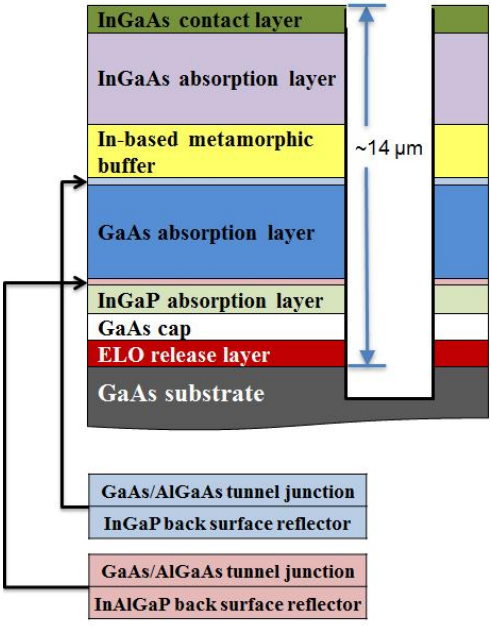

Figure 1. Cross-sectional cartoon of the triple-junction solar cell heterostructure used for via demonstration.

RESULTS AND DISCUSSION

Fig. 2 shows typical SEM images of 20-µm square vias etched into full 4-inch wafers with different gas chemistries. For each chemistry shown, the process parameters (flow rates, gas composition, pressure, RIE and ICP power, and temperature) were adjusted to optimize the etch profile and mask selectivity; only the best identified recipes (as determined by sidewall anisotropy and etch morphology) are shown here. As can be seen in Fig. 2(a), the Cl_2/Ar gas chemistry resulted in significant "grass" along the bottom of the via and substantial sidewall roughness. Different substrate temperatures, gas flow rates and RIE/ICP power levels were evaluated, but none of these process variations were able to improve the morphology appreciably. Replacing Cl_2 with BCl_3 resulted in substantial benefits to the etch profile and sidewall surface smoothness, but at the expense of a 50% drop in etch rate. To improve the etch rate (essential for the formation of deep vias), Cl_2 was mixed with the BCl_3/Ar gases; even a small amount of Cl_2 (6.7%) raised the semiconductor etch rate by about 2 times (to ~440 nm/min). However, the Cl_2-induced sidewall undercut (as can be seen in Fig. 2(b)) was dependent on the In content of the layers in the heterostructure. To further optimize the etch process to achieve composition-independent, smooth etch sidewalls, $SiCl_4$/Ar gas chemistry was investigated. Nearly vertical sidewalls with smooth morphology and clean bottom etch profiles were obtained, as shown in Fig. 2(c). Further, the etch rate was a comparatively high 550 nm/min. Uniformity across the 4" wafer was assessed using laser scanning confocal microscopy. As shown in Fig. 3, etch variation of less than 3% was achieved across a full 4" wafer.

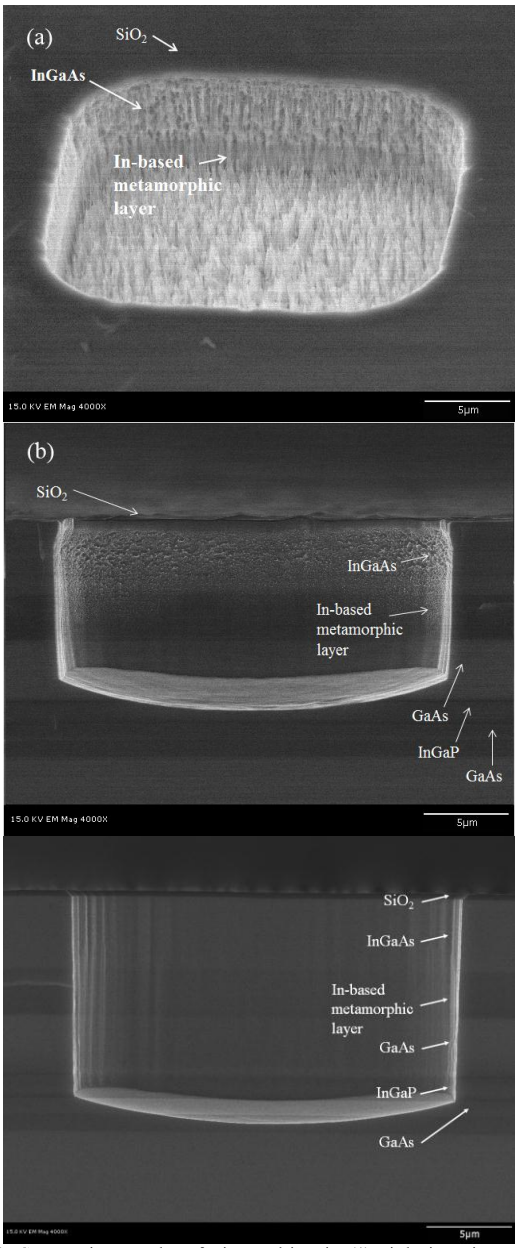

Figure 2. SEM micrographs of vias etching in 4" triple junction solar cell wafers. (a) Cl_2 / Ar = 3 sccm / 12 sccm and 2 mTorr; (b) BCl_3 / Cl_2 / Ar = 10 sccm / 2 sccm / 20 sccm and 3 mTorr; (c) $SiCl_4$/Ar = 5 sccm / 10 sccm and 0.6 mTorr. Other process parameters were: 100 W RIE power, 300 W ICP power, and 180 ºC substrate temperature.

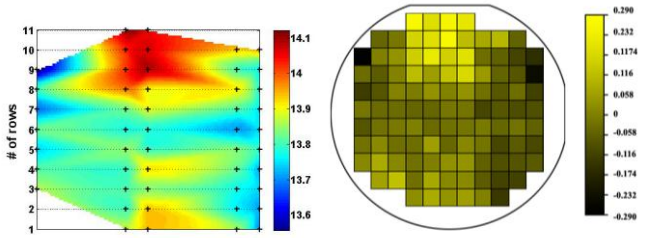

Figure 3. Via depth uniformity on a typical 4-inch wafer for the $SiCl_4$/Ar ICP-RIE process.

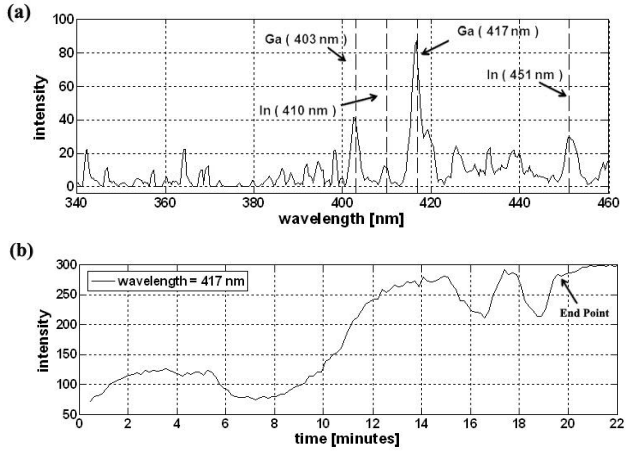

Figure 4. OES spectrum of typical Cl_2 / Ar etch conditions (a) at the start of etching, and (b) a time-scan for the 417 nm peak.

The OES spectra were also recorded as a function of etch time to determine if OES could be effective in monitoring etch progress. Fig. 4(a) shows a typical spectrum (at the start of etching) showing the emission from various species in the plasma, and a time-scan for the 417-nm emission peak (associated with Ga) is shown in Fig. 4(b). As can be seen in Fig. 4(b), very clear indications of the progress of the etch through the heterostructure can be seen due to compositional differences between the various epitaxial layers. Similar time-dependent spectral signatures were observed for other spectral features (e.g., the In-related peaks at 410 nm and 451 nm, and the Ga peak at 403 nm). As can be seen in Fig. 4(b), OES allows real-time tracking of the etch progress through the heterostructure, and appears promising for ensuring robust process control.

The performance of the etch processes on small test samples was compared to the results obtained on full 4" wafers for each of the etch chemistries evaluated, in order to understand if process development could be done with small pieces. The test results indicate that the carrier wafer surface has a significant impact on the etch profile and etch rate for small-sample etching. With SiO_2-coated Si carrier wafers, the results on small samples and full wafers were most similar; using bare Si or SiN_x-coated wafers resulted in significant differences, as determined by inspection by SEM. The OES data also indicate that carrier wafer composition impacts the process. Fig. 5 shows the measured OES spectrum for a full 4" wafer etch, as well as small samples on bare Si and SiO_2- or SiN_x-coated carrier wafers. As can be seen in Fig. 5, the emission spectra during small-sample etching with Si or SiN_x carrier wafers showed significant differences (particularly for wavelengths in the range from 370 to 400 nm) compared to the spectrum obtained from a full-wafer etch process, while using a SiO_2–coated carrier reduced the discrepancy greatly. This suggests that reactions between the etching gases and the carrier wafer influence the ion and radical species and population in the chamber, and thus the carrier wafer must be carefully selected.

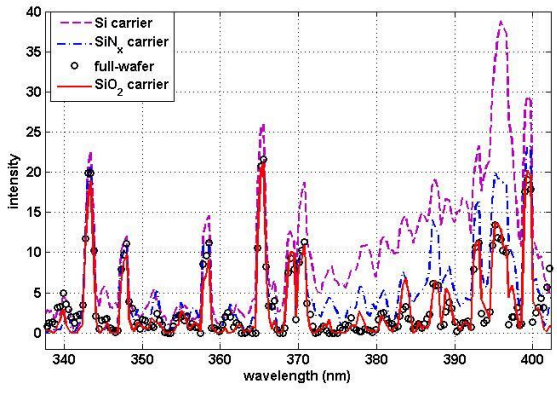

Figure 5. OES spectra during typical Cl_2/Ar etch process on full wafer and small samples with different carrier wafers. Clear distinctions among the carrier wafer types can be observed, particularly for wavelengths from 370 to 400 nm.

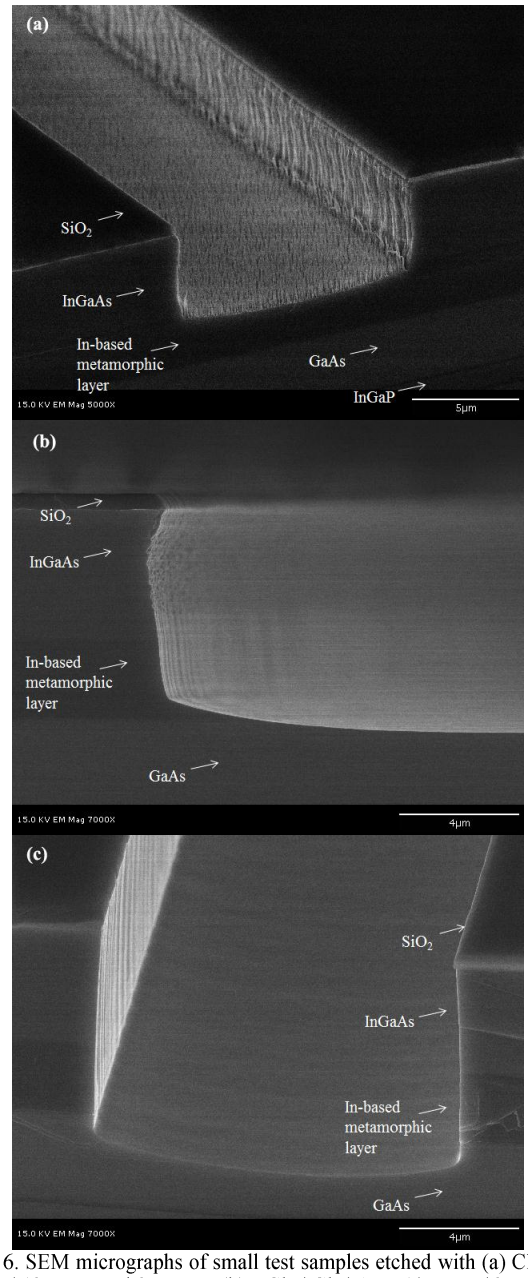

Figure 6. SEM micrographs of small test samples etched with (a) Cl_2 / Ar = 3 sccm / 12 sccm and 2 mTorr, (b) BCl_3 / Cl_2 / Ar = 10 sccm / 2 sccm / 20 sccm and 3 mTorr, and (c) $SiCl_4$/Ar = 5 sccm / 10 sccm and 0.6 mTorr. Other process parameters were: 100 W RIE power, 300 W ICP power, and 180 ºC substrate temperature.

In terms of etch morphology, Fig. 6 shows the results for Cl_2/Ar, BCl_3/Cl_2/Ar, and $SiCl_4$/Ar etching on small samples on a SiO_2-coated Si carrier wafer. The BCl_3/Cl_2/Ar and $SiCl_4$/Ar results are quite similar to the full-wafer etch, while the Cl_2/Ar etch shows much less "grass" for small samples, but with similar sidewall morphology to the full wafer result. This suggests that considerable caution must be exercised in developing processes on small pieces. The key differences between small sample etching and full-wafer etching were attributed to electrostatic and loading effects. Since the

small samples were mounted with thermal grease on a carrier wafer, a non-uniform plasma sheath above the wafer may result, and also the plasma self-bias voltage is distributed differently compared to the full-wafer etch case due to the insertion of the thin grease and carrier wafer into the effective substrate capacitance [2]. In addition, it was observed that etches performed with the SiO_2 carrier wafer exhibited slightly reduced DC bias voltages (V_{dc}); V_{dc} decreased around 7% compared to the V_{dc} of full-wafer etching under identical $SiCl_4$/Ar etch conditions. Loading effects were observed as a shift in etch rate—$SiCl_4$/Ar etching on small samples was found to be approximately 56% faster than on full wafers. To investigate this further, the loading effect was also evaluated for full-wafer etching but with different mask patterns. In Fig. 6, an OES time-scan for the 451 nm Indium peak is shown for two full-wafer etches performed under identical plasma conditions, but with two different pattern densities. In addition to the difference in measured OES signal strength, clear etch rate differences were observed between the two full-wafer etches; the etch rate increased approximately 30% when the exposed semiconductor regions across the wafer was decreased from 3.7 cm^2 to 1.1 cm^2. This clearly indicates the role of both electrostatics and loading in the developed processes, and provides a guide for interpretation of results obtained from the use of small test samples.

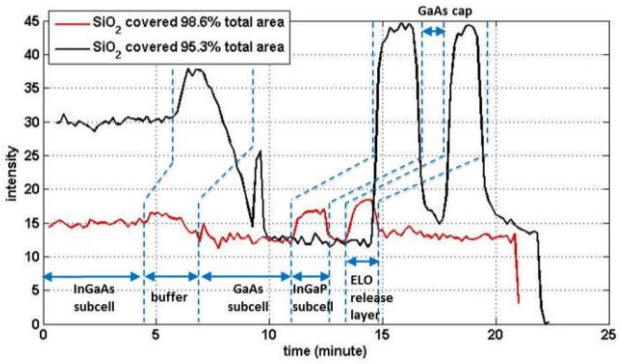

Figure 7. OES time-scan for the 451 nm Indium peak, comparing two identical full-wafer etches but with different mask patterns.

CONCLUSIONS

A comparison of Cl_2/Ar, BCl_3/Ar/Cl_2, and $SiCl_4$/Ar gas chemistries for full-wafer, small-area via-hole fabrication processing has been discussed. Smooth, vertical and uniform etch profiles were obtained on InGaAs/GaAs/InGaP IMM triple-junction backside contact photovoltaic cells, using a $SiCl_4$/Ar-based etch. OES Indium and Gallium emission peaks showed clear signals for real-time process tracking, and some subtleties to be aware of in attempting process development with small samples were discussed.

REFERENCES

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