Achieve Manufacturing Readiness Level 8 of high-power, high efficiency 0.25µm GaN on SiC HEMT Process

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Abstract

TriQuint is in the third year of a Defense Production Act Title III contract to improve GaN manufacturing capability and establish a domestic, economically viable, open-foundry merchant supplier production capability for S-band and wideband MMICs employing GaN epitaxy on 100mm SiC substrates. TriQuint has achieved more than 1E6 hours MTTF at 200◦C channel temperature on production GaN on SiC technology. In Title III program, through improvements in GaN characterization, process variability reduction, and cycle time reduction, TriQuint is working to complete the program with a final manufacturing readiness level assessment of 8. This paper discuss the methodology utilized and observations made during the program.

I. INTRODUCTION

TriQuint is in the third year of a Defense Production Act Title III contract to improve GaN manufacturing capability to meet future military production needs. The benefits of GaN to provide higher power density, improved system efficiency, simplified power distribution and cooling, and ultimately reduced cost have clear advantages in performance for future military systems. GaN has significant advantages over GaAs due to higher mobility, higher breakdown voltage, and higher maximum operating temperature.

The primary objective of the Title III program is to achieve a Manufacturing Readiness Level (MRL) of 8 for manufacturing S-Band and wide bandwidth (X/Ku-band) GaN on SiC MMIC components with a production line ready to support Low-Rate InitialProduction. In addition, the objectives of the Title III program are to establish a domestic, economically viable, open-foundry merchant supplier production capability for narrow and wideband MMICs employing GaN epitaxy on 100mm SiC substrates.

The TriQuint Title III effort builds on a long history of development and manufacturing of GaN MMICs. TriQuint's effort began in 1999 and resulted in the release of a qualified manufacturing process for GaN MMICs on 3 inch SiC substrates in 2008. A 4 inch process was released in 2010 and is in use for standard product development and foundry projects for external customers.

Through the Title III program, TriQuint is making significant progress in achieving the manufacturing maturity needed to serve the needs of future military production programs. TriQuint's approach to achieve the primary program goal of MRL 8 is to establish requirements through Key Performance Parameters (KPPs) for process and MMIC performance characteristics, assess the gaps in the metrics relative to requirements through a baseline Manufacturing Readiness Assessment (MRA) to determine an initial MRL; assess the gaps to MRL 8; improve and refine the process; and finally repeat the MRA to demonstrate MRL 8 capability. The KPPs include process control monitors, MMIC yields, passive components (capacitors), cycle time, cost, and reliability goals. Meeting the reliability goals is one of TriQuint's top priorities.

II. TITLE III PROCESSES AND TECHNOLOGY DEMONSTRATION VEHICLES

The HEMT devices were fabricated from MOCVD-grown epitaxial layers on 100mm c-plane 6H and 4H SI-SiC substrates. The devices were isolated using RIE etching, and the ohmic contacts were formed with alloyed Ti/Al-based metals. The gate-length is 0.25µm defined by e-beam patterning with an integrated field-plate. In addition, a source-connected second field-plate (2FP) was implemented to reduce the high-field related device degradation. The distance from the source to the 2FP was selected to improve the PAE and gain at high voltage. For backside via, the SiC wafers were ground and polished to 100 µm, and the GaN/SiC vias were etched in an ICP-RIE process. Finally, the backside ground plane was plated with Au.

The Title III program is targeting specific MMIC performance requirements. Achieving those requirements required optimization of gate channel features for specific characteristics. Both the S-band performance and the wideband performance capability were optimized through field plate engineering. Subsequently, MMICs were designed to meet the requirements and are in use as demonstration vehicles for the program goals.

The S-band MMIC is a 2-stage power amplifier, that is designed for both high power and Power Added Efficiency (PAE). The wideband PA is designed for power and PAE covering X to Ku-band. Each mask set for the individual amplifiers contains a single stage test circuit, FETs for unit

cell performance assessment, and test structures for FET parametric and process performance assessment. In process measurements from all the structures on the mask sets are used to assess process performance and reliability to the KPPs.

Reliability testing consists of various tests assessing a discrete test FET, a single stage evaluation test circuit (SEC) and the S-Band and wideband MMICs. For DC accelerated life testing, devices with 300-μm total gate periphery were assembled into packages and were stressed in a nitrogen environment at channel temperatures of ~355 ◦C (as estimated by device modeling) with a drain bias of 28V and drain current = 250 mA/mm. During stress, the gate bias was adjusted to keep Id constant at 250 mA/mm. As the stress time progressed, periodic measurements of the maximum drain current (defined as Vd = 5V, Vg = +1V) were taken to assess device degradation. Device failure was considered when the maximum drain current measure degraded >10% and >20%. Single-temperature DC accelerated life testing is done on every program wafer to benchmark reliability, as well as 3-temperarture testing to establish activation energy of every change of process of record. SEC RF operational life testing (OLT) consists of stressing the SEC at a channel temperature of ~150 ◦C at an RF drive corresponding to peak PAE. The SEC is first biased at Vd = 28V and quiescent bias set to 100 mA/mm. Based on dissipated power, baseplate temperature was adjusted to achieve 150 ◦C under RF drive. During RF OLT, input power, output power, drain voltage, drain current, gate voltage, gate current, and baseplate temperature all recorded. Both the SECs and demonstration MMICs are tested for 1000 hours. Degradation is determined by comparing pre and post stress power sweeps at room temperature. A single 8000 hour test is also to be performed on the demonstration MMIC. Reliability achieved to date of TriQuint's GaN technology is mean-time-to-failure (MTTF) of greater that 10 million hours at 200 ◦C channel temperature and MTTF > 1 million hours at 225 ◦C.

Analysis of the data collected in processing the demonstration vehicles is used to drive improvement efforts by determining gaps to the KPP requirements. This is called the Improve and Refine phase of the project. The improvement methodology is executed in three stages: (1) DOE exploration to identify critical variables, (2) confirmation to assess variable interactions, and (3) validation / qualification which is approved through our Technology Review Board. The validation stage uses a minimum of 24 wafers and data collected is used to derive statistical process control limits for continued process monitoring.

III. Approach to Achieve Manufacturing Readiness Level 8

In the Improve and Refine phase, we focused on the following areas: 1) Tightening manufacturing process variability, 2) Implementation of GaN specific characterization and tracking, and 3) Reduction of cycle time. Each experiment to refine the manufacturing technology was first assessed through feasibility runs, then validated the improvements in desired metrics through confirmation runs. Thorough analysis of process monitors, device performance and reliability are executed before qualifying the changes into production. In the next section, key observations that were impacted by process changes, tracking methods unique to GaN production, and cycle time reduction lessons learned will be discussed.

IV. Discussion of Observations and Impact to Manufacturing Technology

Driving root cause to process variability is critical to maturing GaN on SiC manufacturing technology. We successfully identified the source of wafer-to-wafer dependence of the nitride capacitor deposition process. We observed a bimodal distribution in capacitance that was not lot-based but wafer-based (Figure1). We learned that coupling of the wafer to our plasma deposition system resulted in different deposition rate for some wafers. By implementing a process adjustment step when forming the interlayer SiNx layers, Figure 2 showed that the nitride wafer-to-wafer dependence was eliminated, and the capacitance distribution was improved. Thus, the RF performance uniformity of the S-band and wideband MMICs were significantly tightened through disciplined manufacturing approach.

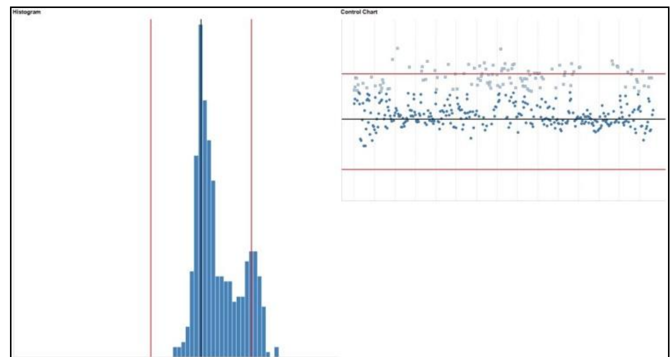

Figure 1. Process A capacitance distribution

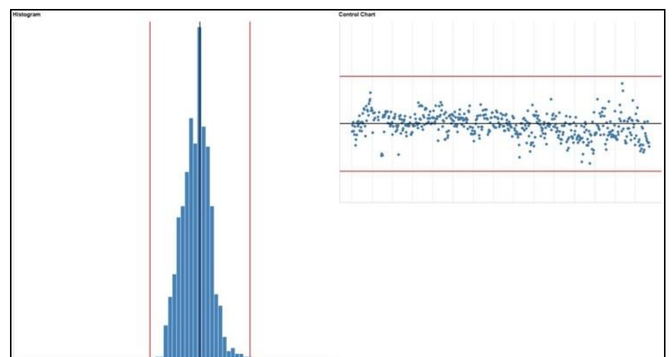

Figure 2. Process B capacitance distribution

We also observed that gate leakage can be impacted by tightening surface conditioning. It is well-known that the GaN device performance is sensitive to surface condition and interactions with the epi layer in the process flow. Figure 3 compares the gate leakage results between two steps during transistor formation. Clearly, from three lots, a change in the process and tools affected the device characteristics and its spread. Design of Experiments (DOEs) were carried out with alternate processes and tools with different capabilities. The new process reduced defects, resulting in consistent wafers. In addition, the selected tool provided automation that greatly improved process control monitoring.

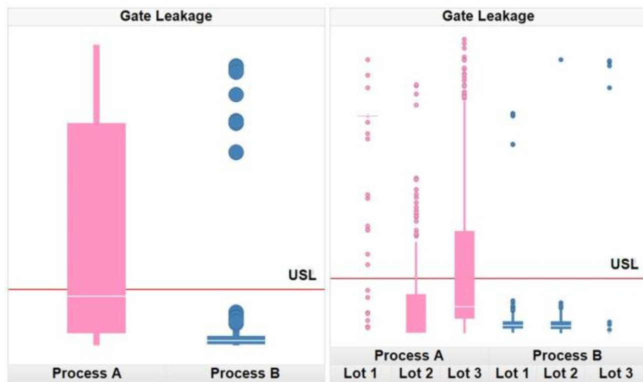

Figure 3. Gate leakage plotted by Process, Process and Lot

In the initial rounds of refine experiments, the impact of the process DOEs at various steps on GaN transistor performance was studied independently. In many cases, such as observations on the capacitors, this approach was successful. In the case of resist removal, TriQuint found improvements in physical cleanliness and significant reduction of process defects with clean changes made at different steps independently in the flow, however, no tightening of electrical parameters were measured over several lots (Figure 4) When the same processes were integrated and performed together in the GaN flow, distinct reduction of the distribution in key electrical parameters was discovered (Figure 3).

GaN on SiC technology requires unique characterization and tracking due to its properties compared to other mature processes. In this section, we will discuss testing and tools TriQuint used to assess and monitor as we go through Improve and Refine phase. An example of a new characterization technique was required was the challenge associated with a clear SiC substrate. A typical optical inspection is unable to detect scratches. As TriQuint is a firm believer in knowing the quality and meeting requirements of starting GaN material, TriQuint has implemented a Candela inspection tool. This additional characterization has allowed for measurement and categorization of defects such as scratches, micropipes, particles, etc. Figure 5 shows an example of the Candela map and what the "trench" found looks like under the microscope. This inspection is used to screen incoming material and return material as necessary. Ongoing work is in progress to establish correlation between device failures and incoming material defects

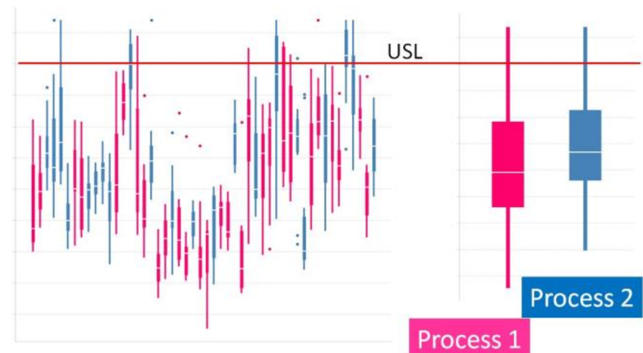

Figure 4. Comparison of gate leakage for process 1 and process 2 over several lots and wafers.

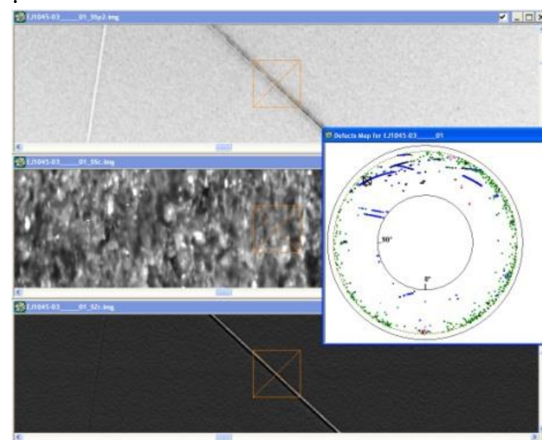
Figure 5. Candela Map and defect magnification.

Another measurement technique specific to GaN that was implemented in production is assessment of current collapse by pulsed IV testing. Current collapse, well-studied trapping phenomenon in GaN, would adversely affect the RF performance and yields in manufacturing readiness improvements. To assess the amount of trapping in the device, first a low trap filling quiescent bias condition of VDS = 0V and VGS = 0V is used to measure the Imax curve. The gate voltage is pulsed from the quiescent bias condition to VGS = 1V while VDS is pulsed from the quiescent bias to different drain voltages ranging from 0V to 20V to map out the Imax curve. The traps are then filled by using a quiescent bias of VDS = 40V, VGS = -6V. Again the gate voltage is pulsed from the quiescent bias condition to VGS = 1V while VDS is pulsed from the quiescent bias to different drain voltages ranging from 0V to 20V to map out the Imax curve (Figure 6). A comparison of these two curves allows determination of the amount of electron trapping in the device. As a metric,1-(ratio of the 2nd IDS curve, pulsing from VDS = 40V and VGS = -6V, to the 1st IDS curve, pulsing from VDS = 0V and VGS = 0V), measured at VDS = 5V is defined as the amount of current

collapse. During Improve and Refine process experiments, pulsed IV mapping was performed to understand the impact to current collapse. Figure 7 compares that a change in the gate formation process affects the amount of drain current that will be available for RF operation. In this example, process B resulted in lowest figure of merit in current collapse tracking, therefore indicating that was a desired process change.

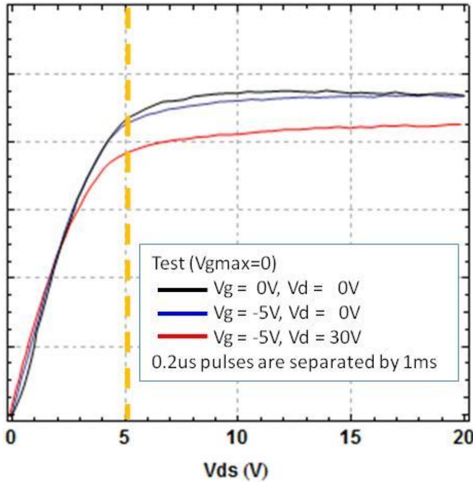

Figure 6. ID curve at Vg=0V comparing pulsed IV sweeps from different starting pulse points.

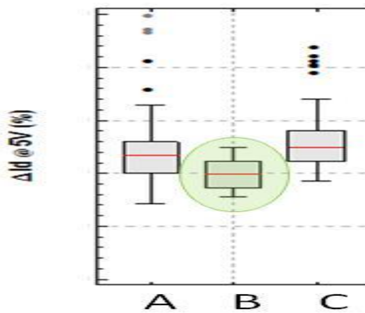

Figure 7. Comparison of pulsed IV results by process.

Cycle time is another performance parameter when measuring the manufacturing readiness level for this program. Since our initial production release, TriQuint has been actively reducing cycle time through fab tool redundancy, elimination of bottlenecks, and tool automation. Through the support of the Title III program, throughput of the SiC/GaN via etch step was increased by qualifying a second etch tool. Through a series of power and pressure optimization experiments, the via etch rate was increased while improving uniformity. Cycle time reduction of 3x was achieved at the via step (Figure 8). Additional cycle time improvement can be realized by moving to a higher throughput process such as from e-beam to optical lithography. For this process change, not only the photo patterning had to be defined. Also investigated was the surface conditioning as influenced by interactions of the resist, developer, and resist removal. In the Title III program, we demonstrated similar performance metrics while improving manufacturability of the GaN flow.

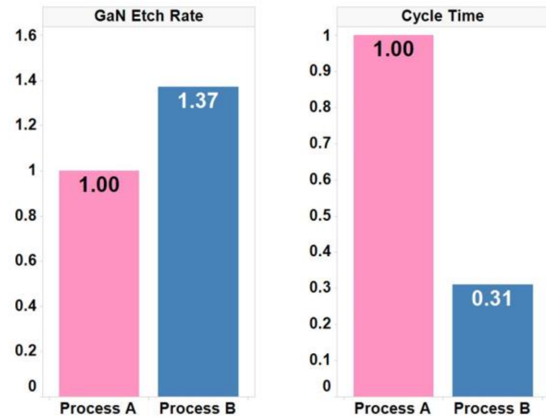

Figure 8. Comparison of source via GaN etch rate and cycle time by Process.

SUMMARY

TriQuint is committed to long-term high-volume, high performance GaN MMIC production. With the support of the Title III GaN program we have made significant progress towards a mature GaN manufacturing technology. Using a disciplined Improve and Refine methodology we have closed the gaps in our key performance parameters through improvements in process variability reduction, GaN characterization, and cycle time. We shall complete the program with final goal of meeting Manufacturing Readiness Level 8.

ACKNOWLEDGEMENTS

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