DARPA's Intra/Interchip Enhanced Cooling (ICECool) Program

Avram Bar-Cohen[1], Joseph J. Maurer[2], Jonathan G. Felbinger[2]

Defense Advanced Research Projects Agency, 675 N. Randolph St., Arlington, VA 22203, ABC@darpa.mil
Booz Allen Hamilton, 3811 N. Fairfax Dr., Arlington, VA 22203, Maurer_Joseph@bah.com

Keywords: thermal management, near junction, intrachip, interchip, GaN, embedded high performance computing

Abstract

The Defense Advanced Research Projects Agency (DARPA) is pursuing research working toward a new paradigm of *embedded* cooling for thermal management of microelectronic devices. This work was initiated in the Near Junction Thermal Transport (NJTT) thrust, which is the transitional effort to an embedded cooling paradigm, building on the advanced remote cooling developed in the Thermal Management Technologies (TMT) program. The full implementation of embedded cooling is being pursued in the two efforts of the Intra/Interchip Enhanced Cooling (ICECool) program: ICECool Fundamentals and ICECool Applications.

BACKGROUND

The increased integration density of electronic components and subsystems, including the nascent commercialization of 3D chip stack technology, has exacerbated the thermal management challenges facing electronic system developers. The confluence of chip power dissipation above 100W, localized hot spots with fluxes above 1kW/cm^2, and package-level volumetric heat generation that can exceed 1 kW/cm^3 has exposed the limitations of the current "remote cooling" paradigm and its inability to facilitate continued enhancements in the performance of advanced silicon and compound semiconductor components. These thermal limitations have compromised the decades-long "Moore's Law" progression in microprocessor performance and threaten to derail the innovation engine which has been responsible for much of the microelectronic revolution.

In conventional cooling architectures for electronics, reliance on thermal conduction and spreading, in the commonly-used chips and substrates and across the multiple material interfaces present in packages and modules, severely constrains the ability of remotely located heat rejection surfaces to reduce the temperature rise of critical on-chip hot spots and individual chips in a module or in a stack. Moreover, continued application of this "remote cooling" paradigm has resulted in electronic systems in which the thermal management hardware accounts for a large fraction of the volume, weight, and cost of advanced electronic systems and undermines efforts to transfer emerging electronic components to portable, as well as other small form-factor, applications.

Thermal Management Technologies (TMT) program

In 2008 DARPA initiated the Thermal Management Technologies (TMT) program to address these thermal management challenges by reducing the overall thermal resistance associated with the prevailing "remote cooling" paradigm. The TMT program includes several distinct efforts to utilize emerging micro- and nano-technology for enhanced thermal performance and these efforts are now coming to fruition, with considerable success [1].

The Microtechnologies for Air Cooled Exchangers (MACE) effort seeks to develop heat sinks which utilize flow agitators, synthetic jets, compressed air, and fins with integral heat pipes to reduce the thermal resistivity towards 10 cm^2 K/W, meaning a 10 Kelvin temperature rise for a heat flux of 1 W/cm^2, with a fan coefficient of performance (COP) approaching 30. The Thermal Ground Plane (TGP) thrust is developing high-performance "vapor chamber" heat spreaders in which micro–nano biporous wicks, some with hydrophobic–hydrophilic surfaces and expansion-matched cases, can provide in-plane thermal conductivities between 10kW/mK and 20kW/mK, or 25-50 times higher than copper and more than 10 times higher than synthetic diamond. Enhanced thermal interface materials, based on mechanically-compliant laminated solder-graphite, GLAD fabricated copper nanosprings, and arrays of carbon nanotubes (CNTs), respectively, that could accommodate the differential expansion between silicon and copper while reducing the thermal resistivity to below 0.01cm^{2}K/W for a 0.1mm thick layer, are resulting from the NanoThermal Interfaces (NTI) thrust. Miniature high-efficiency refrigeration systems, based on thermoelectric or Sterling cycle technologies that can be inserted into the chip stack-up and capable of reaching COPs of 2 for a 15K temperature reduction under an applied heat flux greater than 25W/cm^2, are being pursued under the Active Cooling Module (ACM) effort.

Near Junction Thermal Transport (NJTT)

Despite considerable success in TMT and on-going evolutionary improvements in COTS thermal packaging

7
a

technology, the sequential conductive thermal resistances inherent to the “remote cooling” paradigm have resulted in only limited improvements in the overall junction-to-ambient thermal resistance of high-performance electronic systems during the past decade. To overcome these limitations and remove a significant barrier to continued “Moore’s Law” progression in electronic components and systems, it is essential to directly cool the on-chip heat generation sites and extract the dissipated heat with microfluidic flow through the chip, substrate, and/or package. Integral liquid cooling, involving dielectric liquid flow through the chassis, “tray” and/or mounting surfaces for high power components, has already demonstrated benefits in both computing and RF applications, for example as described in [2] for the IBM Power 775 Supercomputer, in [3] for an RF array, and in [4] for a single MMIC. Continuation of this trend with *embedded* microfluidic thermal management will overcome thermal limitations, as well as the SWaP bottleneck, and can be expected to transform electronic system architecture in next-generation defense electronic systems.

The Near Junction Thermal Transport (NJTT) thrust initiated DARPA’s efforts in the creation of this new *embedded* cooling thermal management paradigm. NJTT is attempting to reduce the thermal resistance of the near-junction region (the first 100 µm) of microelectronic devices, without reducing electrical performance. NJTT is thus establishing a dividing line between the limits of the current “remote cooling” paradigm and the emergence of an integrated, embedded cooling paradigm.

NJTT is focused on approaches that will allow GaN PAs to operate in existing DoD systems with significant increases in power handling and without accompanying increases in the temperature difference from the junction to the base of the heat sink or cold plate, deleterious effects on the electrical characteristics, or incompatibilities in material sets or fabrication processes. NJTT teams are not altering the electrical design of the PAs, but rather are pursuing thermal management approaches, such as high conductivity materials or liquid cooling, that can substantially reduce or remove the thermal barriers to high-power operation of GaN PAs and similar components.

NJTT, an 18–24 month program, began in late 2011.The specific teams and their approaches are as follows: BAE Systems, Raytheon IDS, RFMD, and TriQuint Semiconductor are exploring epitaxial transfer of GaN onto high conductivity diamond substrates. Northrop Grumman AS is exploring direct growth of diamond into thermal vias etched in the SiC substrate of the GaN. The final NJTT team, GE Global Research, is exploring single-phase cooling of a GaN on SiC PA with microchannels etched into the SiC substrate within 50 µm of the GaN.

Additionally, NJTT has a strong focus in metrology and modeling to address the challenges of measurement verification at the sub-micron scale and quantifying thermal–electrical performance of the GaN devices. At the end of the program, the teams will demonstrate the improved power handling of their techniques.

Intrachip/Interchip Enhanced Cooling (ICECool)

DARPA’s Intrachip/Interchip Enhanced Cooling (ICECool) program picks up where NJTT left off and is focused on fully implementing the new embedded cooling paradigm. ICECool will explore disruptive thermal technologies that will mitigate thermal limitations on the operation of military electronic systems, while significantly reducing size, weight, and power consumption (SWaP). A conceptual ICECool chip is shown in Figure 1. The overarching vision for ICECool is to place thermal management on an equal footing with functional design and power delivery and utilize embedded thermal management to enhance the performance of military electronic systems.

ICECool will involve the creation of a rich micro/nano grid of thermal interconnects, using high thermal conductivity – as well as thermoelectric – materials to link on-chip hot spots to convectively and evaporatively cooled microchannels. Such intra/inter chip enhanced cooling approaches will need to be compatible with the materials, fabrication procedures, and thermal management needs of emerging homogeneous and heterogeneous integration in 3D chip stacks, 2.5D constructs, and planar arrays.

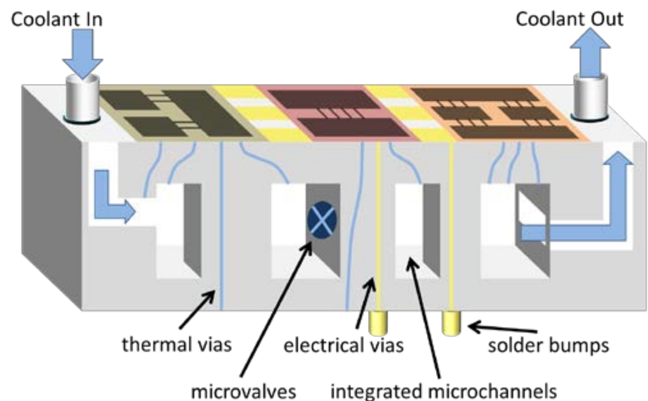

Figure 1: Conceptual ICECool chip

An intrachip approach, depicted in Figure 2, would involve fabricating micropores and microchannels directly into the chip [5, 6] while an interchip approach, shown in Figure 3, would utilize the microgap between chips in three-dimensional stacks [7] as the cooling channel. In addition to the inclusion of an appropriate grid of passive and/or active thermal interconnects, it is expected that a combination of

intrachip and interchip approaches, linked with thru-silicon and/or "blind" micropores will confer added thermal management functionality. These microchannels and/or micropores will need to be integrated into a fluid distribution network, delivering chilled fluid to the chip and extracting a mixture of heated liquid and vapor to be transported to the ambiently cooled radiator. Moreover, on-chip microvalves – thermostatically or digitally controlled – will be needed to regulate the flow of the coolant and assure the most efficient use of its latent and sensible cooling capacity. The ICECool program consists of two related thrusts: ICECool Fundamentals and ICECool Applications.

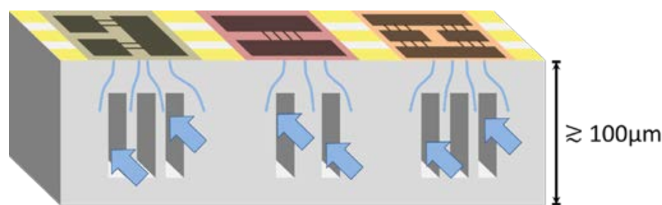

Figure 2: Conceptual ICECool intrachip approach

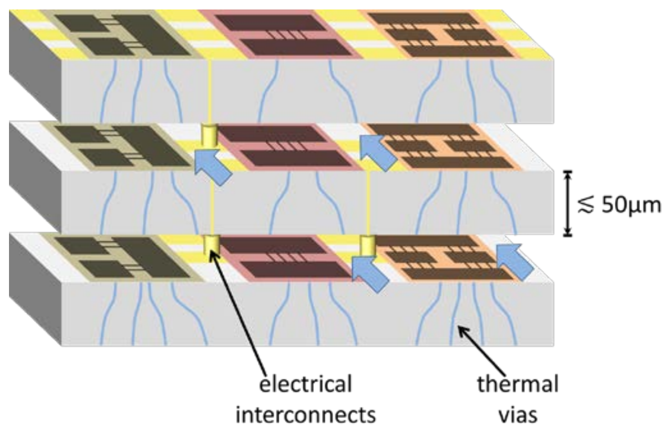

Figure 3: Conceptual interchip approach

ICECool Fundamentals (ICECool Fun)

The goal of ICECool Fun is to demonstrate chip-level heat removal in excess of 1 kW/cm^2 heat flux and 1 kW/cm^3 heat density with thermal control of local submillimeter hot spots with heat flux exceeding 5 kW/cm^2, while maintaining these components in the usually-accepted temperature range of the chosen candidate application by judicious combination of intra- and/or interchip microfluidic cooling and on-chip thermal interconnects. ICECool Fun is, thus, the first step toward achieving the system performance goals of the ICECool program and will develop the fundamental building blocks of intrachip and interchip evaporative microfluidic cooling. ICECool Fun will, over an anticipated 24–36 months, develop and demonstrate the microfabrication techniques needed to implement thermal interconnects and evaporative microfluidics in multiply-microchanneled semiconductor chips and study, model, and correlate intrachip heat diffusion and the thermofluidic characteristics of evaporative flows in microchannel flow loops within individual chips and/or in the microgaps between chips in 3D stacks.

ICECool Fun performers will fabricate and deliver an intra- or interchip cooled demonstration vehicle embodying the ICECool techniques as selected by the individual team. Performers will address the following areas as part of their ICECool Fun effort:

- Model-based design and fabrication of stable, high exit quality evaporative microfluidic cooling systems capable of providing a minimum 1 kW/cm^2 heat flux and 1 kW/cm^3 heat density removal across a chip and/or chip stack without exceeding commonly accepted process and device operating temperature limits.
- Design, fabrication, and implementation of boiling initiation and localization measures.
- Microfabrication of high aspect ratio microchannels and/or micropores in a relevant electronic material (Si, SiC, or diamond) as well as integration of micro-"fittings," such as microvalves, micropores, and fluid connectors, as needed.
- Incorporation, along with evaporative microfluidics, of thermal management techniques, such as high conductance on-chip thermal interconnects and vias, on-chip thermoelectric coolers, and thermal architectures that enable remediation of a uniform, 200×200 µm on-chip hot spot, exceeding heat fluxes of 5 kW/cm^2, at the center of the chip within uniformly-heated (1 kW/cm^2) surroundings.
- Model-based parametric study of the thermal transport characteristics of the proposed approach and the study of the feasibility of exploiting these mechanisms for integrated/embedded thermal management of operational electronic devices and the deleterious effects that might result.
- Characterization of the thermal performance limits and physics-of-failure of the proposed high heat density, on-chip, cooling technologies.

ICECool Applications (ICECool Apps)

The ICECool Applications program will sponsor 30-month design, development, and demonstration efforts involving intrachip/interchip thermal management, through microfluidic flow with sufficiently dielectric liquids and on-chip active and/or passive thermal interconnects. ICECool Apps proposals are solicited in two distinct Technical Areas:

- RF MMIC PAs: Technical Area I relates to the thermal management needs of GaN RF MMIC power amplifiers, targeting die-level heat fluxes of

1kW/cm^2 and HEMT (sub-millimeter "hot spot"), heat fluxes of 30kW/cm^2 or greater, while providing package-level heat removal density of greater than 2kW/cm^3.

- Embedded HPCs: Technical Area II addresses the cooling needs of embedded high performance computer modules; targeting chip heat fluxes of 1kW/cm^2 and sub-millimeter macrocell "hot spots" with heat fluxes up to 2kW/cm^2, while providing a chip stack heat removal density of 5kW/cm^3.

ICECool Applications will produce a thermal management paradigm change in defense electronic systems, leading to greater performance of COTS MMICs, CPUs, GPUs, and FPGAs and to reduced system SWaP. ICECool Apps performers will define and demonstrate intrachip and interchip thermal management approaches that are tailored to one of these specific applications and this approach will be consistent with the materials sets, fabrication processes, and operating environment of the intended application. Moreover, in the interest of achieving near-term system insertions of ICECool Apps technology, proposers will apply embedded microfluidic thermal management techniques to existing liquid-cooled systems, in which the external thermal management hardware (pumps, valves, heat exchangers, etc.) can be harnessed in an ICECool-driven design. ICECool Applications efforts will, thus, culminate with successful demonstration of enhanced device and module performance. Removal of the thermal and SWaP bottlenecks on existing COTS components is anticipated to underpin the design and development of high-performance next-generation defense electronic systems that transcend COTS components.

CONCLUSIONS

DARPA's Embedded Cooling portfolio of programs (i.e., NJTT, ICECool Fundamentals, and ICECool Applications) is establishing a new *embedded* thermal management paradigm where aggressive cooling is built into the chip, substrate, and/or package to directly cool the heat generation sites. NJTT is targeting significant reductions in the near-junction thermal resistance and on-chip hot spot temperatures in wide band gap MMIC power amplifiers through the transfer of GaN epitaxial layers onto diamond substrates and engineering of the epitaxial transition layers. ICECool Fundamentals is pursuing the discovery and technology development needed to underpin the implementation of evaporative two-phase microfluidic cooling and create the building blocks for interchip and intrachip application of this highly efficient thermal management technique. Most recently, ICECool Applications is pursuing near-term insertion of single phase embedded microfluidic cooling targeting existing liquid-cooled RF and high performance computing systems.

ACKNOWLEDGMENT

The authors acknowledge the support of the government team and the outstanding achievements of the performers who are involved in DARPA's TMT and ICECool programs.

Disclaimer: The views, opinions, and/or findings contained in this article/presentation are those of the author/presenter and should not be interpreted as representing the official views or policies, either expressed or implied, of the Defense Advanced Research Projects Agency or the Department of Defense.

Distribution Statement A, Approved for Public Release, Distribution Unlimited.

REFERENCES

1. A. Bar-Cohen, K. Bloschock, "Advanced thermal management technologies for defense electronics," Proceedings, SPIE Defense, Security and Sensing Conference, Baltimore, MD, April 2012.
2. G.F. Goth, A. Arvelo, J. Eagle, M.J. Ellsworth, K.C. Marston, A.K. Sinha, J.A. Zitz. "Thermal and Mechanical Analysis and Design of the IBM Power 775 Water Cooled Supercomputing Central Electronics Complex." *13th IEEE ITHERM Conference*, pp. 700-709, 2012.
3. S. Holzwarth, O. Litschke, W. Simon, H. Fischer, J. Kassner, A. Serwa. "Highly Integrated 8x8 Antenna Array Demonstrator on LTCC with Integrated RF Circuitry and Liquid Cooling." *EuCAP 2010*, Barcelona, April 2010.
4. J.P. Calame, R.E. Myers, F. N. Wood, and S.C. Binari. "Simulations of Direct-die-attached Microchannel Coolers for the Thermal Management of GaN-on-SiC Microwave Amplifiers." *IEEE Transactions on Components and Packaging Technologies*, 28.4, pp. 797-809, 2005.
5. D.B. Tuckerman and R.F.W. Pease. "High-performance heat sinking for VLSI." IEEE Electron Device Letters, vol. 2, no. 5, pp. 126–129, 1981.
6. L.P. Yarin, A. Mosyak and G. Hetsroni. Fluid Flow, Heat Transfer, and Boiling in Micro-Channels. Springer, Berlin, 2009.
7. A. Bar-Cohen, J. Sheehan and E. Rahim. "Two-Phase Thermal Transport in Microgap Channels - Theory, Experimental Results, and Predictive Relations." Microgravity Science and Technology, pp. 1–15, Sept. 2011

ACRONYMS

DARPA: Defense Advanced Research Projects Agency
NJTT: Near Junction Thermal Transport
TMT: Thermal Management Technologies
ICECool: Intra/Interchip Enhanced Cooling
MACE: Microtechnologies for Air Cooled Exchangers
COP: Coefficient of Performance
TGP: Thermal Ground Plane
GLAD: Glancing Angle Deposition
CNT: Carbon Nanotube
NTI: NanoThermal Interface
ACM: Active Cooling Module
RF: Radio Frequency
MMIC: Monolithic Microwave Integrated Circuit
PA: Power Amplifier
SWaP: Size, Weight, and Power
HPC: High Performance Computer