Ultra Fast Switching Speed FET Technology Development

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Abstract

The creation of a pHEMT FET technology with ultra fast switching speeds is enabling switch and attenuator products that meet the stringent timing requirements of time division based cellular standards. The ultra fast switching speed FET development effort required the characterization of the effects of epi, process, and FET layout configuration on FET switching speed. The factors were then optimized to create a FET that can reach 90% RF power in less than 10ns, and near 100% power in less than 20ns.

INTRODUCTION

Traditional LTE and WCDMA cellular data standards use frequency division (FD), which utilizes separate bands for transmitting and receiving data. Advantages of frequency division include improved spectral efficiency and there is simultaneous transmitting and receiving of data which eliminates the need to guard band the time periods between uplink and downlink transmissions.

Time division (TD) technology utilizes a single frequency with different time periods for transmitting and receiving data. Time division is advantageous when uplink and downlink data transmissions are not symmetric, which is typical for most cellular phones. Time division frequency spectrum also tends to be less expensive. A primary disadvantage of TD technology is the need to have a time guard band between uplink and downlink transmissions. Products that utilize time division standards require switches and attenuators that have fast switch speeds.

The switching speed of pHEMT FETs is strongly influenced by surface trapping mechanisms. Traps are present in the bulk as well as the surface regions of FET devices, but it is believed that surface traps have a more significant effect on FET switching speeds due to their proximity to the active channel. Surface traps can act as a transient negative surface charge which depletes the free carriers in the underlying n-type material and increases the resistance of the device[1]. The level of traps is a function of the applied Vgs condition and affects the transient performance of a FET as shown in figure 1.

When a pHEMT FET is turned from the off to the on state, the depletion region directly under the gate is immediately reduced, but transient depletion regions in the access areas of the device are present which diminishes as the surface de-traps. This transient depletion region causes the conductance of the FET to increase with time creating what is commonly known as gate lag.

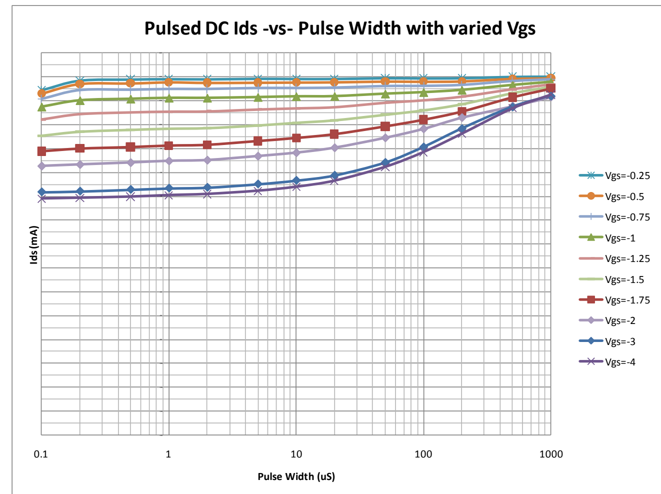

Figure1. *Pulsed IV Id-vs-pulse width at varied Vgs pulse levels at -20 °C*

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EXPERIMENTAL METHODS

Many design of experiments (DOE) were run to assess the effects of factors on gate lag. To better assess the effects of factors, some DOEs were run using epi and/or processes with known high trap densities, while others were run with lower known trap density epi and/or processes. The resultant devices were measured over temperature using a dIVA D225EP under worst case bias conditions to assess the effects of each factor on gate lag. Measurements on attenuator circuits were also performed on-wafer using the difference in attenuation level (insertion loss) measured at 200ns and 5ms as an indicator of switch speed.

The primary gate lag factors that were evaluated are epi doping, epi composition, epi layer thicknesses, un-gated recess dimension, pre-passivation treatment methods, silicon nitride passivation deposition conditions, and FET layout configuration. Multiple variables were evaluated within each potential gate lag factor.

Experimental Results

The design of experiments and device characterizations were performed over a number of years. The pulsed IV and on-wafer measurements strongly indicate that most of the variables that were evaluated affect gate lag and switch speed.

A variety of epi DOEs were performed where the composition, doping level, and thickness of different epi layers were varied. The effects of epi layer thickness and doping on pulsed IV performance is shown in Figure 2. To best understand the effects of these epi factors, this DOE was fabricated using a known higher trap density wafer fabrication process. The results indicated that changes in epi design will reduce the gate lag effects of surface traps.

Experiments were performed where the gate level process was altered to produce un-gated recess dimension with varied dimensions. Figure 3 shows the pulsed IV response of these varied un-gated recess conditions. To best understand the effects of this factor, the experiment was performed using a known high trap density process. The data indicates that gate lag is affected by this variable, with the largest un-gated recess condition having the highest gate lag.

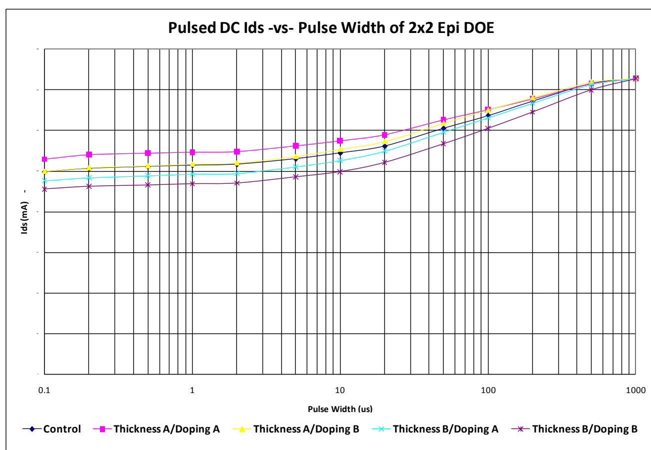

Figure2. *Room temperature pulsed IV response of epi doping and epi thickness factors using high trap density fabrication process*

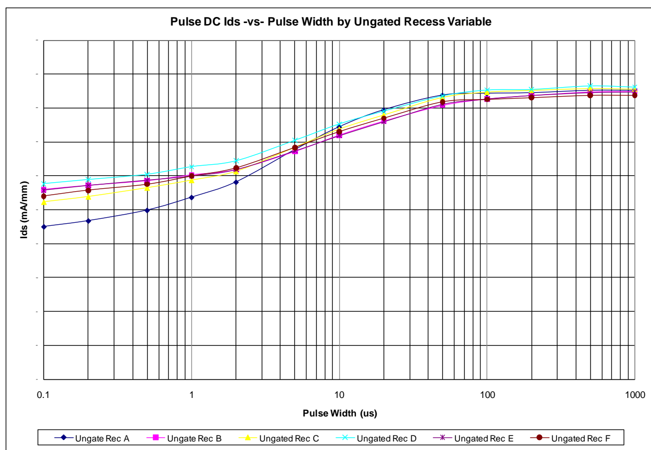

Figure3. *Room temperature pulsed IV response of varied un-gated recess conditions using high trap density fabrication process*

Pre-passivation cleaning experiments were also performed using wet chemistry, plasma clean, and hybrid wet/plasma cleaning techniques. Figure 4 shows the affects of pre-passivation treatment methods on pulsed IV response. The pre-passivation cleaning process clearly affects gate lag, but is only apparent at pulse widths of less than 5us.

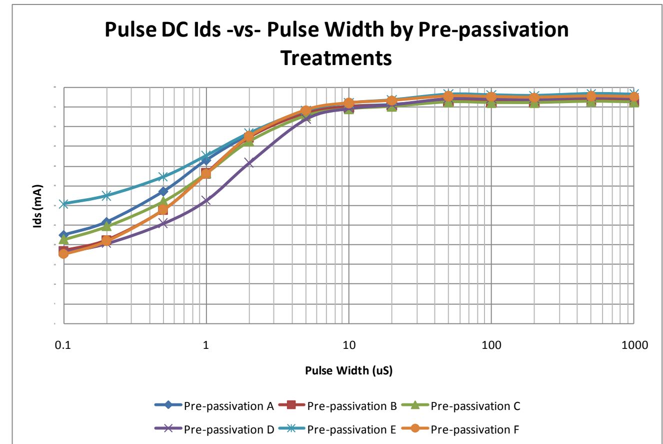

Figure4. *Room temperature pulsed IV response of by pre-passivation treatment method*

Passivation deposition DOEs were also performed with varied process conditions. The process gas flow rates, process gas ratios, power levels, and timing were varied to assess the effects of these factors on device performance. Figure 5 shows the affects of passivation nitride deposition factors on pulsed IV performance. This experiment was performed using an improved epi and lower trap density fabrication process at prior operations. The process conditions used for silicon nitride passivation deposition strongly affected gate lag. The data may suggest that the silicon nitride passivation deposition process conditions can create traps with time constants at room temperature of greater than 1ms. It also indicates that minimal gate lag can be achieved with a well characterized epi design and wafer fabrication process. The present ultra fast switch speed FET is a derivative of the epi and process conditions used to fabricate passivation A devices from figure 5.

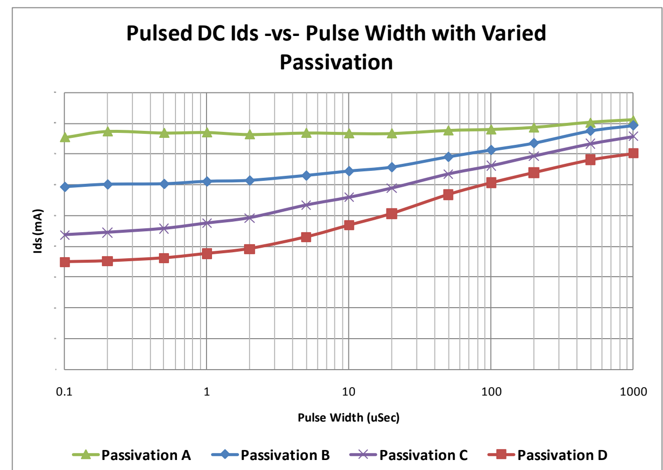

Figure5. *Room temperature pulsed IV response by passivation method using improved epi, and lower trap density fabrication process*

Devices were also pulsed IV tested over temperature conditions ranging from -20C to +85C. Figure 6 shows the normalized Ids over temperature of the ultra fast switching speed FET. The data was normalized to the DC Ids of the

85C measurement and then scaled across different pulse widths. The 10,000us data points on the chart are actually the measured DC Ids of the device. There are minimal differences in gate lag across this temperature range for the ultra fast switch speed FET with it being only slightly more dispersive at -20C.

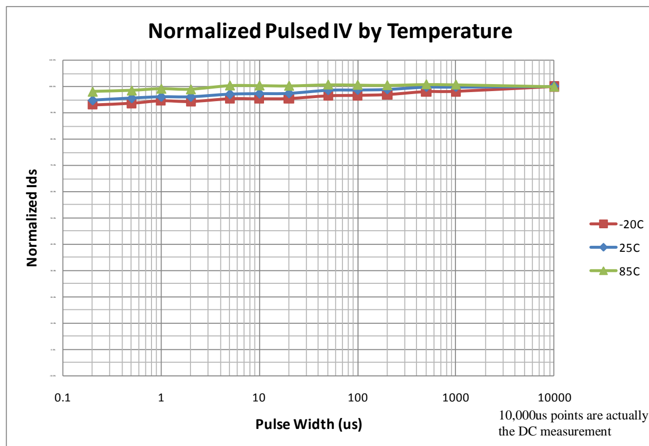

Figure6. *Normalized pulsed IV response by temperature of present ultra fast switch speed FET at Vgs pulsed from -5V to 0.5V and Vds pulsed from 0 to 0.5V*

PRODUCT RESULTS

A design of experiments was also run to better understand the effects of FET and circuit design configurations on the switch speed of circuits. A series/shunt single bit attenuator was used for this evaluation which is shown in figure 7. Resistors R1 and R2 determine the attenuation level of the circuit, while R3 is for impedance matching. Different FET types (number of gates/FET and number of FETs in series) as well as capacitor and gate resistor values were evaluated on both the series and shunt portions of the test circuit. The attenuation levels of the circuits were tested using an engineering on-wafer prober. The prober was set up to measure the attenuation level (insertion loss) in 50ns increments from 500ns prior to the series FET being 'turned-off' and shunt FET 'turned-on' until 5ms after this event. The difference in attenuation level from 700ns point (200ns after series FET turned off) and 5ms after this event was calculated and is used as an indicator of switch speed.

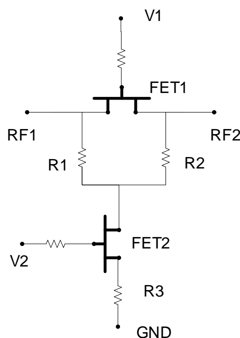

Figure7. *FET and circuit design element switch speed test circuit*

The on-wafer test data from over 9,000 devices fabricated with the ultra fast FET process is shown in figure 8. There is a clear effect of circuit design on switch speed. FET configuration, capacitor and resistor values have a meaningful affect on the overall switch speed.

An example of the switching speeds being attained using the ultra fast switching speed FET on a single pole, two throw circuit is shown in figure 9. The green lines indicate the timing of the gate bias voltage of each arm, while the orange lines indicate the insertion loss levels of each arm. This circuit reaches 90% power in less than 10ns, and near 100% power in less than 20ns.

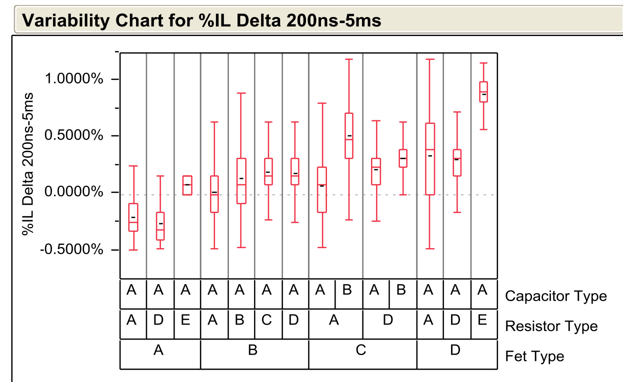

Figure8. *Percent difference in insertion loss between 200ns and 5ms of design configuration DOE measured at RF on-wafer test.*

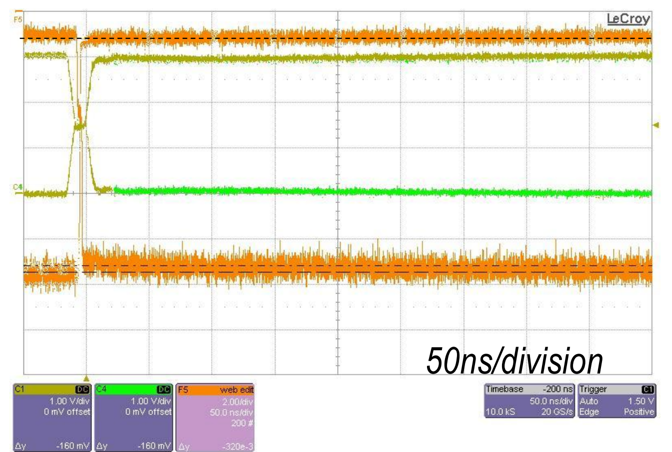

Figure9. *Single pole two, throw pHEMT circuit switch speed. Green lines are the gate bias voltage conditions for each arm. Orange lines are corresponding RF response of each arm in dBm.*

Conclusions

Device performance requirements and characteristics will evolve with time. Over temperature pulsed IV measurements are a valuable tool for characterizing the transient performance of FETs. It was used in conjunction with many epi, process, and design experiments to better understand factors that affect the gate lag and switch speed of devices and circuits. The effort resulted in an ultra fast switch speed pHEMT FET that supports customer performance requirements.

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engineering lots. We are also grateful for the assistance of Tom Fenwick and the on-wafer test team for developing an on-wafer test stand capable of making the necessary transient measurements, and using this stand to measure numerous engineering wafers.

REFERENCES

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ACRONYMS

DOE: Design of Experiments
FET: Field Effect Transistor
HBT: Heterojunction Bipolar Transistor
LTE: Long Term Evolution
pHEMT: Pseudomorphic High Electron Mobility Transistor
WCDMA: Wideband Code Division Multiple Access