Process Improvements for an Improved Diamond-capped GaN HEMT Device


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Abstract

Diamond has been proposed as an integrated heat sink layer for Gallium Nitride (GaN) high electron mobility transistors (HEMTs). The NRL “Gate after diamond” approach has demonstrated 20% reduction in self-heating. The second generation of this process implements diamond directly on GaN to serve both as a passivation layer and to increase the heat spreading effect. A sacrificial gate process is also added to produce a more reliable gate opening without damaging the GaN by ICP etching.

INTRODUCTION

As a wide-bandgap semiconductor, gallium nitride (GaN) is attractive for next-generation power converters. The capabilities of GaN-based high electron mobility transistors (HEMTs) to date have been limited by the self-heating effect (reduction of drain current due to lower carrier mobility caused by increased phonon scattering at high drain fields), which has been well-documented in the literature [1-3]. However, attempts to alleviate it have been limited.

Nanocrystalline diamond (NCD) thin-film growth technology has advanced significantly in recent years [4,5]. NCD films possess unique properties, notably high thermal conductivity (up to 1300 W/m-K for t_{NCD} > 3 µm) and very small grain size (~5 nm). Such properties have enabled the growth of smooth (5-25 nm RMS roughness) layers that can act as heat spreading device capping layers. Such schemes in GaN involve growth of AlGaN/GaN on single crystal [6] or CVD [7] diamond, or capping of fully-processed HEMTs using NCD [8], [9]. The bottom-side diamond approaches have faced limitations with substrate size and wafer bow management, while top-side heat extraction using diamond capping of fully-processed AlGaN/GaN HEMTs mandates lower growth diamond temperature, and thus a lower thermal conductivity, due to the presence of a thermally sensitive Schottky gate [8].

EXPERIMENTAL

We have previously reported improved electrical performance and a 20% reduction in channel temperature with a “gate after diamond” process, which enables large-area, high thermal conductivity top-side diamond without damaging the Schottky gate [10]. In the first generation of this device, the diamond was deposited on a thin nucleation dielectric (10 nm PECVD SiN_x) after the mesa and ohmic steps have been completed, but before the gate metal. An O_2-based etch is used to clear the diamond in the gate region before metal deposition. Details of this fabrication sequence can be found elsewhere in the literature [7].

There are several drawbacks to this process flow. Most significantly, the passivation layer/nucleation dielectric, however thin, acts as a thermal insulator between the hottest part of the device and the heat spreading layer. In addition, the plasma etch for the gate opening produced significant micromasking and plasma damage to the gate region of the device. To solve these problems, we have improved the diamond nucleation and initial growth processes to enable diamond deposition directly on the device surface, modified the plasma etch to reduce damage, and investigated a sacrificial gate process to make the gate opening step more reliable. A schematic and FIB cross-section of the second generation device is shown in Figure 1.

![Figure 1. Schematic of AlGaN/GaN HEMT with NCD heat spreading film (top) and FIB cross-section (bottom)](image)
RESULTS

The gate opening step is most critical, and requires the most optimization. This step has been performed using an O$_2$/Ar (40/15 sccm) ICP etch at 10 mT with 800W ICP power and 300W RIE power. While the etch rate for NCD is quite high in this process (~180 nm/min), an etch stop layer is necessary. It became clear that as we made the nucleation dielectric thinner to bring the diamond closer to the active region of the device, the etch stop was not sufficient to prevent damage to the channel, which is manifested by a decrease in mobility and 2DEG density as shown in Table I. This becomes even more critical when moving to a process that eliminates the nucleation dielectric. In addition, the process creates a significant amount of micromasking, as shown in Figure 2 (top). To eliminate the micromasking, the ICP and RIE power were reduced (keeping the ratio the same) as far down as 100W ICP/30W RIE. The result was a 10X reduction in etch rate, but no change in the degree of micromasking. It was hypothesized that the features were not actually micromasking but a region of higher quality diamond – essentially the nanodiamond was etching from grain boundaries, but the high quality diamond at the center of each crystal was not etching. The features did not affect device performance in a power HEMT geometry with a relatively large gate length, but in a scaled RF device this is catastrophic because the density of these crystals will actually prevent the gate metal from contacting the device. By migrating the process to a different ICP etch tool, the features were removed, shown in Figure 2 (bottom). The precise nature of these features is still unclear.

<table>
<thead>
<tr>
<th>TABLE I</th>
<th>Hall Measurements on NCD-Capped HEMTs</th>
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<tbody>
<tr>
<td></td>
<td>$R_{SH}$ ($\Omega/q$)</td>
</tr>
<tr>
<td>Reference</td>
<td>533</td>
</tr>
<tr>
<td>After NCD</td>
<td>553</td>
</tr>
<tr>
<td>After Gate Etch</td>
<td>1.72x10$^{6}$</td>
</tr>
</tbody>
</table>

The results of this etch study were used to develop a 2-step etch to mitigate a significant amount of plasma damage. The high power etch component is employed to remove the majority (~80%) of the diamond film thickness, and the lowest power condition is used to approach the device surface. Devices that were processed with this etch showed significant improvements in mobility and 2DEG density after the gate opening – it was essentially unchanged from the reference level. This process is still not foolproof, however. The diamond process produces a thickness gradient across the sample, with the film being thinnest at the center and up to 100nm thinner at the edge of the sample. The etch process is much more uniform, therefore a gate opening that is timed to stop precisely at the device surface at the center will naturally overetch at the edge. Therefore a new process is required.

A sacrificial gate process was developed to perfect the gate opening step. In this process flow, a sacrificial gate finger is formed before diamond. Following diamond growth, the gate feature is realigned and the diamond etch is used to clear the NCD with a thick etch stop layer. The sacrificial finger is removed in a wet etch that will not damage the GaN, followed by gate metal alignment and lift-off. The sacrificial finger was formed in a stack of 20nm ALD Al$_2$O$_3$/1 µm SiN$_x$. Given the line widths and aspect ratios for this feature, an anisotropic plasma etch is necessary to etch the SiN$_x$ layer (SF$_6$ RIE, 50 mT, 44W). Again to prevent damage to the GaN surface, the oxide layer was introduced as an etch stop, as it can easily be wet etched in BOE without significant attack to the other materials. As shown in Figure 3 (top), the subsequent NCD growth is highly conformal to the feature. While selective diamond growth everywhere except the feature would be an ideal solution, this technology is not currently possible. The subsequent realignment and etching will be performed on a stepper to minimize alignment error, and NCD etching follows the previously outline procedures using a single step etch since the damage at the bottom is not a concern. This results in a much more reliable opening since the window for overetch is much larger. A second SiN$_x$ layer is used as a hard mask for the etching, and a BOE soak is used to remove the SiN$_x$ finger to expose the GaN surface. As figure 3 (bottom) demonstrates, the feature clears without micromasking or plasma damage to the gate region. This process flow has been proven, but active HEMT devices have not been fabricated to date.
The key feature in this device is the diamond heat spreading film. It is critical that the heat spreading film be placed as close to the hot spot of the device, but not have any adverse effect on device performance. To this end, the concept of the nucleation dielectric was first proposed to ensure passivation of the device surface, both to prevent current collapse and to protect the HEMT from damage and etching in the NCD growth process, which employs high temperature and high density H₂/CH₄ microwave plasma. However, to move the heat spreading layer closer to the channel, we have removed this passivation layer. By altering the NCD nucleation and initial growth steps, we were able to successfully grow diamond without damaging the HEMT, as shown in Table I. The transfer curves shown in Figure 4 indicate low gate leakage and no Vₜ shift relative to a reference device. The saturation current is low, which can be attributed to the device being finished with non-optimized gate opening processes, thus there is a region of high resistance under the gate. Pulsed I-V measurements taken in a Dynamic I-V Analyzer (DIVA) tool indicate that the NCD films passivate the HEMT surface as well as SiNx films, as shown in Figure 5. Current collapse is quantified by taking a pulsed I-V measurement, followed by a DC measurement, which will have current collapse effects. The decrease in DC I_DS,MAX relative to pulsed conditions is referred to as the current collapse ratio. Furthermore, the reduced negative slope in the 10-20V region for the diamond-capped device can be taken as an indication of reduced self-heating.

![Figure 3. FIB cross-sections of sacrificial gate test structure after NCD deposition (top) and after gate realignment and etching (bottom)](image)

![Figure 4. Transfer curves for NCD-capped HEMT with diamond directly on GaN](image)

![Figure 5. Current collapse on NCD-capped and SiNx-passivated HEMTs, quantified by decrease in DC I_DS,MAX relative to pulsed conditions](image)
CONCLUSIONS

NCD capping of AlGaN/GaN HEMTs has demonstrated a 20% reduction in channel temperature. Process refinements are currently being incorporated to optimize the heat spreading effect and improve reliability. Diamond has been grown directly on GaN to eliminate the thermal barrier presented by the thin passivation layer, and new gate opening processes have been implemented to reduce damage to the device in this critical step. Preliminary results indicate that diamond is an excellent passivation layer alone, and a sacrificial gate process can be used to reliably form a gate opening without damaging the 2DEG. Second generation devices are currently being fabricated with the refined process.

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REFERENCES


