GaN HEMTs for Power Switching Applications: from Device to System-Level Electro-Thermal Modeling

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Abstract

This work describes a comprehensive approach to thermal and electro-thermal modeling of GaN HEMT devices and circuits for power switching applications, and shows how thermal modeling can assist manufacturing and design all the way from the semiconductor to the hybrid power converter.

INTRODUCTION

While still expanding in the microwave arena, GaN HEMTs are making their way into the field of high-power switching thanks to their advantages in terms of power handling and switching frequency [1]-[5]. Since power applications demand strenuous attention to thermal aspects, GaN HEMT thermal modeling has attracted increasing attention over the last few years [6]-[14], but mostly in the field of microwave devices and circuits. Power converters are complex, hybrid systems, and thermal modeling cannot be confined to the device domain: it has to cover all domains, from the device to the package, the heat sink, and finally the board on which the switches are assembled with passive components, freewheeling diodes, etc. [15]. This global approach to thermal modeling is not commonly seen, but as companies enter the market of GaN-based switching converters, it will become strategic for manufacturers and users. This work applies this range of modeling techniques to GaN high power switches and power converters.

DEVICE-LEVEL THERMAL SIMULATION

The first step in the thermal modeling deals with the semiconductor die. Here all available data on geometry and physical structure, material properties, etc., can be used to develop a physical die model; since the device layout has always a modular structure, it is sufficient to model a basic cell representing the elementary building block the switch is made of. At this level, thermal modeling is most efficiently carried out using Finite-Element (FE) tools. We used Comsol Multiphysics as a FE solver throughout this work. A simulation of the 5-finger basic cell of a much larger GaN HEMT switch is shown in Fig. 1. Top metals and pads, source via hole, and die-attach (DA) layer are included in the model.

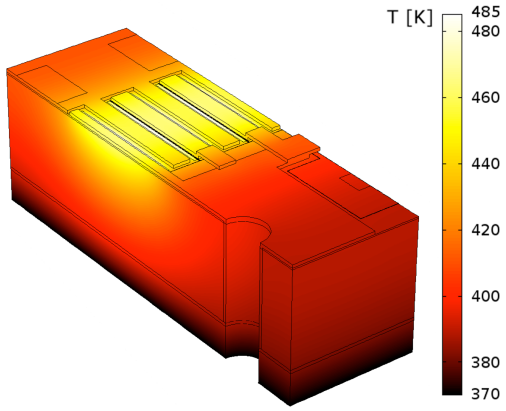

Fig. 1 FE thermal simulation of the basic cell (5x200 μm) of a power GaN switch. The back-side temperature is 370 K. The dissipated power density per unity gate width is 2.5 W/mm. The surface pads are adiabatic (worst-case).

The following data have been used for these simulations:

- Gate finger length/width: 1 μm/200 μm;
- Source/Drain finger length: 27 μm;
- Gate-Source/Gate-Drain spacing: 1μm/12 μm;
- GaN layer thickness: 2.5 μm;
- Silicon substrate thickness: 150 μm;
- Die-attach layer thickness: 50 μm;
- Backside Au layer thickness: 5 μm;
- Source/drain Au metallization thickness: 5 μm;
- Gate Au metallization thickness: 0.5 μm;
- Via external diameter/Au thickness: 70 μm/5 μm;
- Backside temperature T_{AMB}: 370 K;
- Si thermal conductivity: $148 \cdot (300/T)^{1.3}$ W/(m·K);
- Si specific heat/density: 710 J/(kg·K)/2329 kg/m^3;
- GaN thermal conductivity: $160 \cdot (300/T)^{1.3}$ W/(m·K);
- GaN specific heat/density: 490 J/(kg·K)/ 6150 kg/m^3;
- DA thermal conductivity: 45 W/(m·K);
- DA specific heat/density: 227 J/(kg·K)/7300 kg/m^3;
- Au thermal conductivity: 318 W/(m·K);
- Au specific heat/density: 128 J/(kg·K)/19320 kg/m^3;
- GaN/Si thermal boundary resistance: $3.3 \cdot 10^{-8}$ m^{2}K/W.

Simulations like that of Fig. 1 are useful not only in the device design, but also as a guide for the development of compact models for circuit-level simulation.

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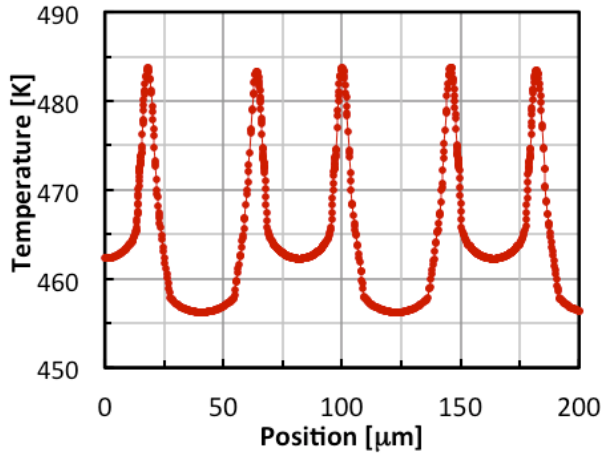

Fig. 2 Simulated T across the GaN HEMT cell in Fig 1. P_D = 2.5 W/mm. The coolest areas are the source contacts. The back-side is at 370 K.

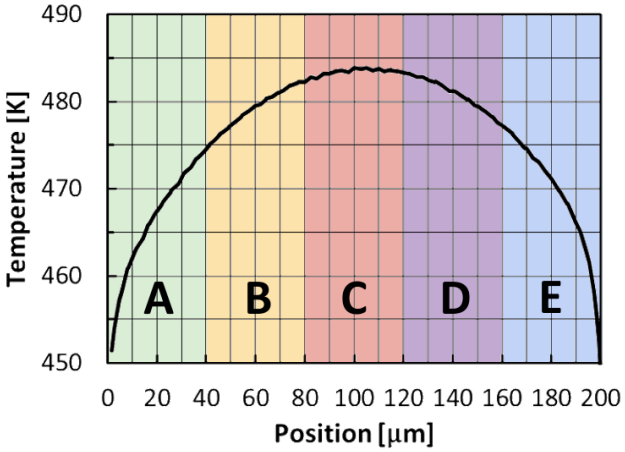

Fig. 3 Simulated T along the 200 μm width. P_D = 2.5 W/mm. The gate width is divided into slabs A-E for LE modeling. The back-side is fixed at 370 K.

For example, while the temperature distribution does not vary much from finger to finger (Fig. 2), it can hardly be considered uniform along the gate finger (Fig. 3). Therefore, in the development of a Lumped-Element (LE) thermal model we partition the structure along the gate width into 5, 40 μm-wide slabs (A-E, Fig. 3), each associated with its channel T, so that an independent Electro-Thermal (ET) model can be extracted for each of them. Our LE modeling approach uses Foster and Cauer 3-stage networks [14]. LE models can be extracted from the FE (or measured) HEMT thermal dynamics, with known algorithms [14] (Fig. 4); the Cauer network parameters are in Tab. I.

Circuit-Level Electro-Thermal Simulation

Once these accurate LE thermal models are available for the A-E slabs, they can be inserted in a self-consistent model (Fig. 5) for physics-based circuit-level ET simulation of power converters.

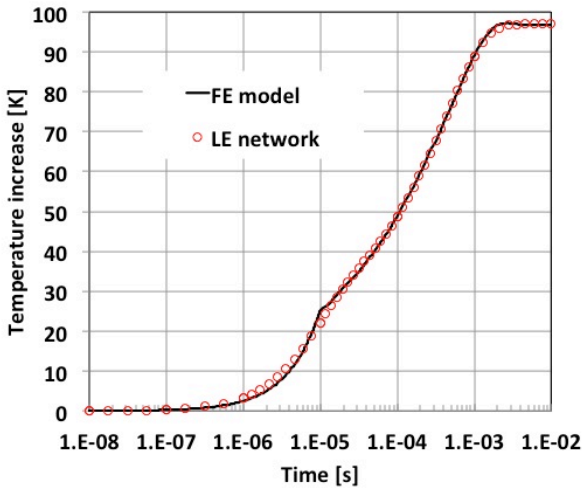

Fig. 4 FE and LE simulation of the ΔT in the A slab (Fig. 3) of the HEMT switch cell of Fig. 1 following a power step of 2.5 W/mm. The LE model is a 3-stage RC network.

TABLE I
LE Cauer Thermal Network Parameters (0.04 mm Gate Width).

Slab	Rθ1 [K/W]	Cθ1 [nJ/K]	Rθ2 [K/W]	Cθ2 [nJ/K]	Rθ3 [K/W]	Cθ3 [nJ/K]
A	340	29	318	393	312	1150
B	386	27	351	293	361	1050
C	394	27	362	266	385	993
D	385	27	345	294	384	955
E	345	28	316	400	352	924

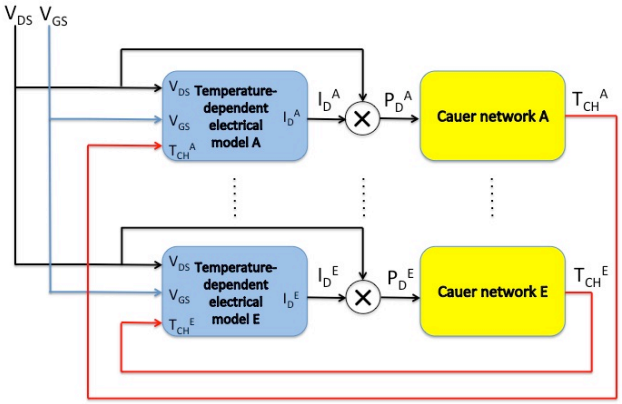

Fig. 5 Self-consistent GaN switch ET model. The 5 electrical models describe the A-E gate slabs in Fig. 3.

Here we opted for a simple model where the HEMT is modeled as a switch with on-state conductivity:

$$G(T) = G_0 (1 - \alpha \Delta T), \quad (1)$$

where ΔT is the T increase over the backside.

We applied the model of Fig. 5 to the simulation of the DC/DC boost converter of Fig. 6. Inside each HEMT block the electrical model is self-consistently coupled with its own LE thermal network (Fig. 5); since the 5 LE networks have different thermal R's and C's (Tab. I), the model can

account for T non-uniformities along the channel width (Fig. 3). The HEMT is described as a switch with on-state resistance R_{ON} (12 mm) = 1.67 Ω (0.139 Ω/mm); therefore the conductance of the blocks in Fig. 6 is G_0 = 0.12 S, while $\alpha = 3\times10^{-3}$ K^{-1} (eq. 1). The other circuit parameters (Fig. 6) are: V_dc = 180 V, L1 = 112 µH, R = 0.2 Ω, D1 V_{ON} = 0.85 V, D1 R_{ON} = 0.32 Ω, C1 = 0.66 µF, I_dc = 1.3 A, f = 1 MHz, 50% duty cycle (360 V output). The peak switch current and dissipated power (Fig. 7) are I_P (12 mm) = 3 A (250 mA/mm) and P_{dP} (12 mm) = 17.5 W (1.48 W/mm), the average dissipated power is <Pd> = 6.5 W (0.54 W/mm).

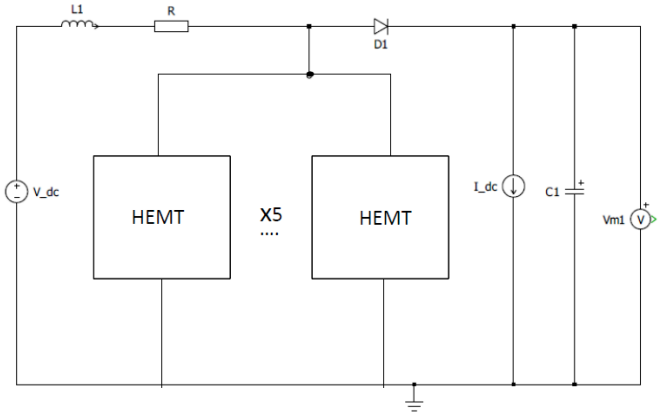

Fig. 6 The modeled DC/DC boost converter. Each HEMT blocks is one of the 5 slabs (A-E) into which we partitioned the cell of Fig. 1 and models a 2.4 mm periphery switch.

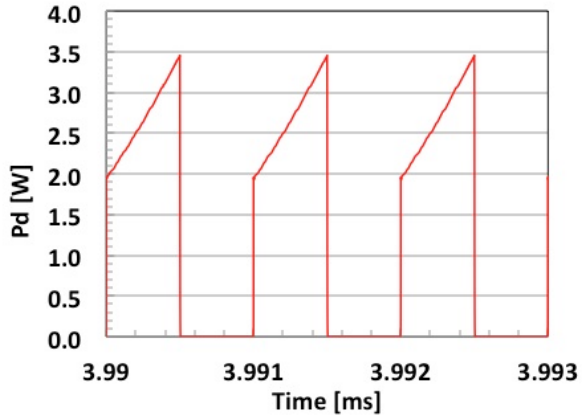

Fig. 7 Instantaneous dissipated power in one of the 5 HEMT blocks in the DC/DC boost power converter of Fig. 6.

Fig. 8 shows T on the hottest (C) and coolest (A) device slabs: the thermal capacitance keeps T nearly constant in the 1 µs cycle; the difference between the hottest and the coolest slabs is about 15% of the average ΔT. Since we derived our LE model from the structure in Fig. 1, the T in Fig. 8 must be added to that of the backside. The HEMT backside is thermally connected to a flange, package and some heat-sinking device (like the converter board itself), but at the switching frequency these external elements sit at a constant T due to their large thermal capacitance.

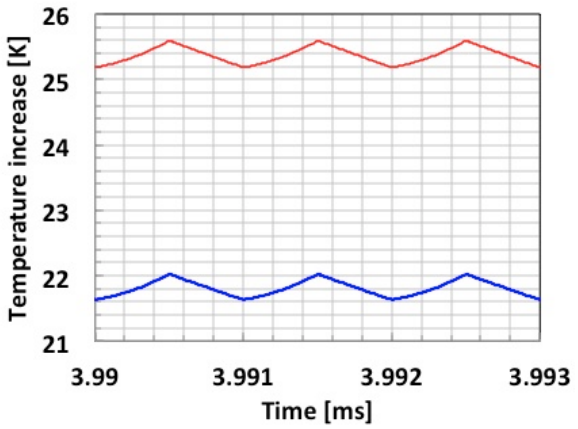

Fig. 8 Temperature increase (over the backside temperature) of the hottest (C) and coolest (A) HEMT blocks in the DC/DC boost power converter of Fig. 7.

The next section shows how this boundary condition can be evaluated.

CIRCUIT-LEVEL (PHYSICAL) THERMAL SIMULATION

Thermal interaction among the converter components can be studied by 3D FE simulations of the whole system [16], the first step of which is obtaining accurate but simple FE models of the individual components, particularly those contributing most heat dissipation, such as the switches. These models must be simple enough to be inserted into the 3D model of the converter without overburdening the computation. Several parameters determining the thermal behavior of the chip/die-attach/package assembly are often unknown, so experimental model tuning is mandatory. Fig. 9 shows the FE model of a commercial packaged GaN power switch; the thermal simulation of the chip and carrier assembly is in Fig. 10. Fig. 11 shows the infra-red (IR) thermography map. The simulated and measured T at different locations (Fig. 10) is reported in Tab. II.

With the individual device models we build a FE model of the whole system, such as the DC/DC Point-Of-Load converter of Fig. 12, to be compared with the corresponding IR map in Fig. 13.

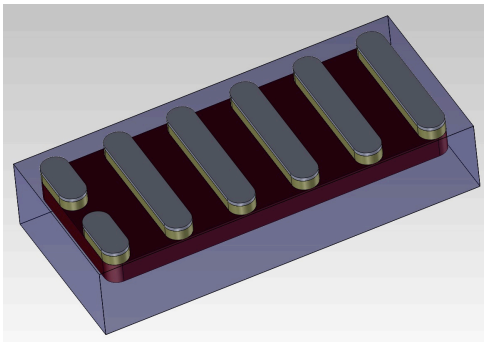

Fig. 9 3D FE model of a packaged GaN HEMT switch.

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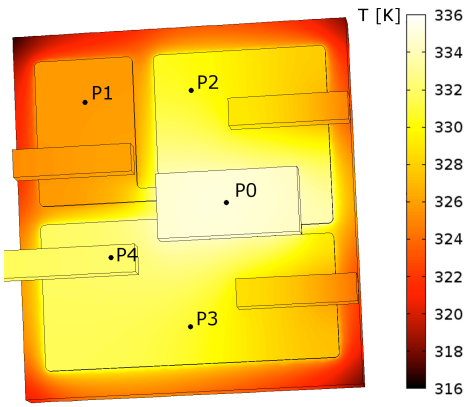

Fig. 10 FE simulation of the GaN switch+carrier assembly. The switch dissipates 1.3 W and is 41 K above ambient.

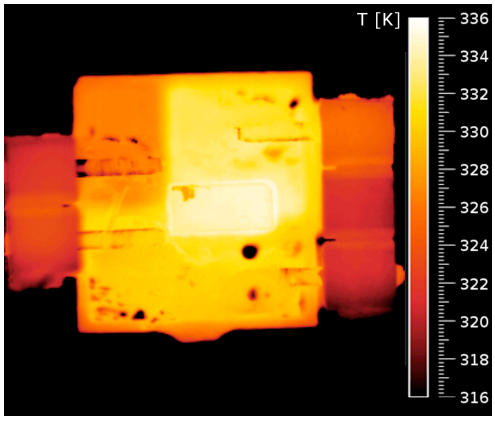

Fig. 11 IR map of the system in Fig. 10. The GaN switch reaches a temperature 41 K above ambient.

TABLE II
SIMULATED AND MEASURED T'S (FIGS. 10 AND 11)

Location	T (simulated) [K]	T (measured) [K]
P0	335	334
P1	326	327
P2	330	332
P3	331	330
P4	332	330

From the validated thermal model of the converter, we can then extract the thermal boundary conditions the switch encounters during operation, and complement the data provided by the electro-thermal model described in the previous section for a complete and realistic assessment of the device behavior and estimated reliability.

CONCLUSIONS

We described a comprehensive approach to thermal and electro-thermal modeling of GaN HEMT devices and circuits for power switching.

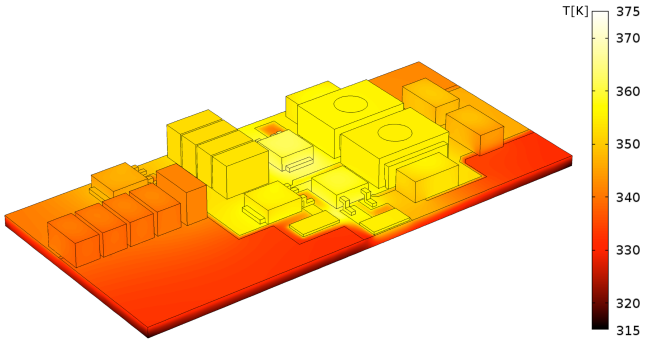

Fig. 12 3D FE thermal simulation of a DC/DC power converter board. The hottest switch dissipates 0.93 W (13% of the whole converter) and is 60 K above ambient.

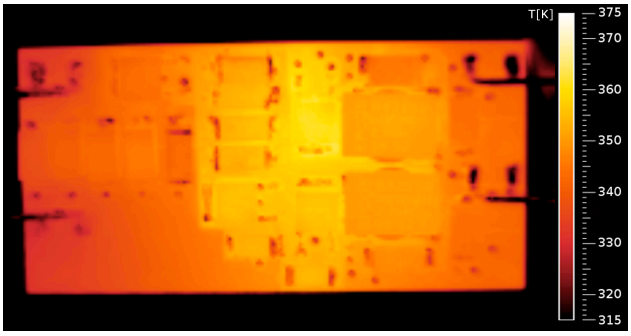

Fig. 13 IR map of the DC/DC power converter simulated in Fig. 12. The hottest switch is 60 K above ambient.

Using commercial simulators and ad-hoc self-consistent electro-thermal switch models, coupled with infra-red thermography measurements, we showed how thermal modeling can assist manufacturing, design and reliability engineers all the way from the physical structure of the GaN switch to the final power converter hybrid circuit.

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ACRONYMS

DA: Die-attach
ET: Electro-thermal
FE: Finite Element
HEMT: High Electron Mobility Transistor
IR: Infra Red
LE: Lumped Element