InGaP/GaAs HBT Safe Operating Area and Thermal Size Effect

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Abstract

Deeply understanding HBT thermal characteristics and safe operating area (SOA) is critical to the improvement of the ruggedness and reliability of power amplifiers. In this work, we investigate the device size effect of SOA and thermal resistance by means of experimental measurement, analytical modeling and 3-dimensional simulation. For HBTs with a factor of ten variations in emitter area, the SOAs are characterized under extremely high current density, and the thermal simulations are performed and the thermal resistances are measured with a thermal-electrical method. It is found that with increasing device size, the SOA in terms of current density shrinks and thermal resistance per unit area increases, which is demonstrated by both simulation and measurement.

INTRODUCTION

InGaP/GaAs heterojunction bipolar transistors (HBTs) have become a major technology in wireless power amplifiers (PAs). As PA die size keeps shrinking, the size of HBT unit cell is of interest and higher operating current density or higher power density may be desirable. On the other hand, PA ruggedness and junction temperature become more of a concern as power density increases. Safe operating area (SOA) that is normally used for the ruggedness characterization at device level has been recently studied [1, 2], but the relationship between the device size and SOA has not been well investigated. Thermal effect is one of the key factors in SOA evaluation [3]; therefore the device thermal characteristics with respect to emitter area also need to be well studied. In this paper, for the first time we report the SOAs with current density over 100kA/cm^2 for different device sizes and explain a new high current density phenomenon with analytical modeling. The results of the thermal simulation and thermal-electrical measurement for various device sizes are also reported, revealing the same size effect as found in the SOA measurement.

SOA MEASUREMENT AND MODELING

The standard TQHBT3 process [4] is used for the wafer fabrication. The unit cell device has two emitter fingers and each finger has nominal width of 3μm and various lengths from 5μm to 50μm. Emitter areas are 2×3×5μm^2, 2×3×10μm^2, 2×3×20μm^2, 2×3×30μm^2, 2×3×40μm^2, and 2×3×50μm^2 respectively. Typical ground-signal-ground (GSG) pads are used for probing and there is no intentional ballasting resistor. A Keithley 4200-SCS parameter analyzer is used for the measurement.

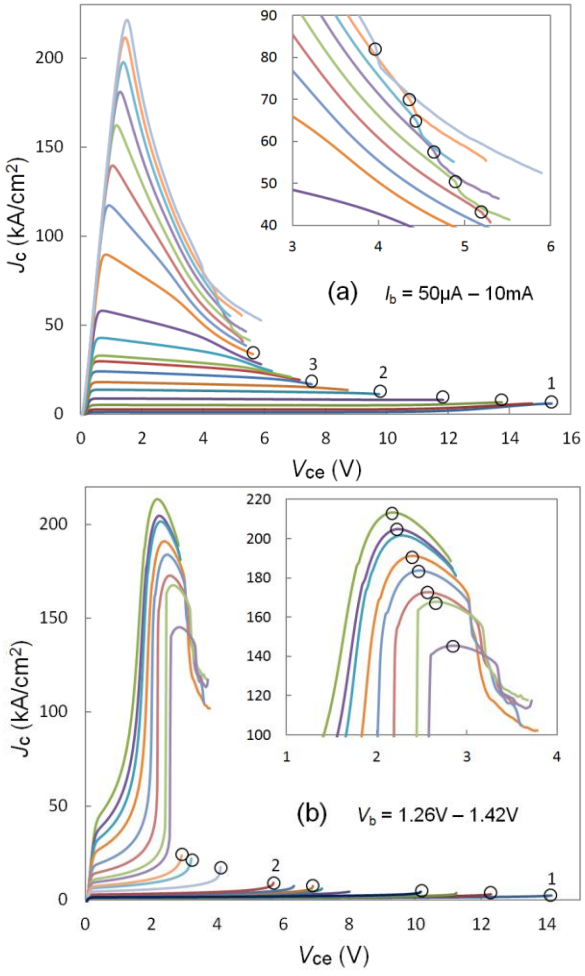

Fig. 1. Measured collector current density versus collector voltage with stepped I_b (a) and stepped V_b (b) for the device size of 2×3×50μm^2. The insets are enlarged plots for the high current density curves and the circles are the points used to define the SOA boundary.

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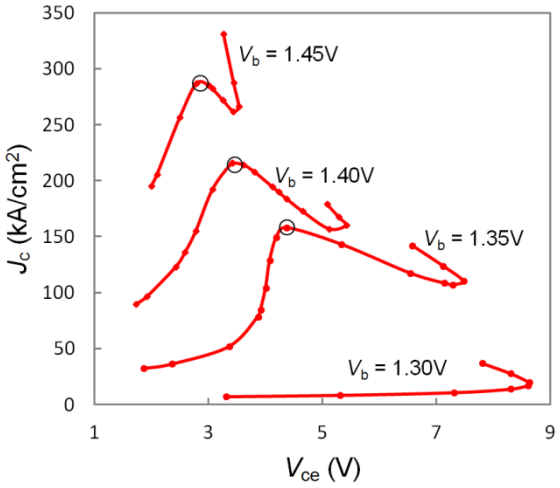

Fig. 2. Calculated IV curves for the V_b mode using analytical models show the exactly the same high current density phenomenon as found in the measurement.

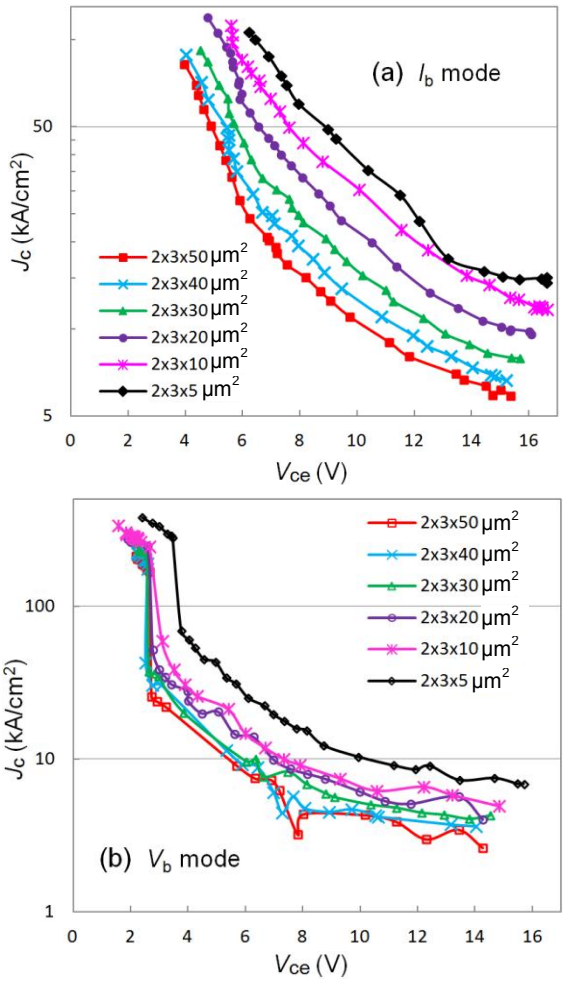

Fig. 3. Measured SOA boundaries with I_b mode (a) and V_b mode (b) for various device sizes (shown in legend).

The measurement is based on common emitter configuration and involves two base bias modes: forcing current (I_b mode) and forcing voltage (V_b mode). For each base bias step, the collector voltage V_c is swept from zero up to the point where the device completely fail, while the collector current I_c is monitored. The device failure mostly exhibits a snap-back of the collector current [5]. Since the test is destructive, a large number of devices are measured across the wafer to obtain one SOA for each emitter size. In doing so, the data has included the variation on the wafer. As an example, Fig. 1(a) and (b) show the measured collector current density (J_c) versus collector voltage (V_c) with I_b and V_b modes for the device of 2×3×50µm^2.

Both I_b and V_b modes exhibit two régimes based on different current behaviors: low current regime and high current regime that is magnified in the inset of Fig. 1 (a) and (b) each. In order to define the loci of points which define the SOA boundary, we use different criteria for these two regimes.

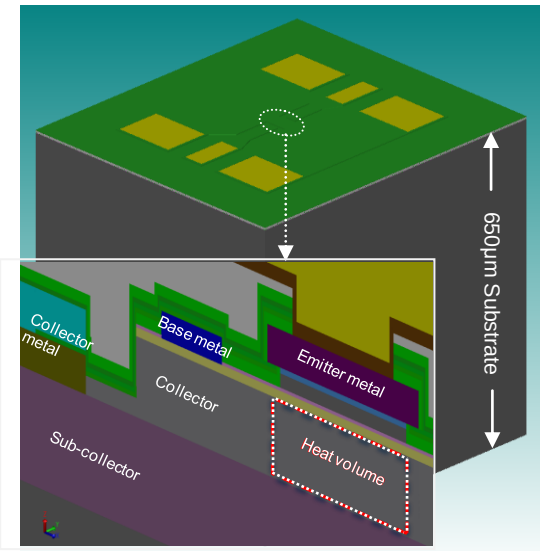

Fig. 4. 3D model for the thermal simulation of a typical HBT unit cell. A cross section of the intrinsic device (dot-circled) is also shown in the lower picture.

In Fig. 1(a), when I_b begins at very low level and the dissipated power is low, J_c saturates until high V_c then increases with sweeping V_c due to impact ionization, and eventually, avalanche occurs at the point (as denoted circle 1) where J_c exhibits a snap-back (not shown); At higher I_b levels, J_c keeps decreasing with increasing V_c in the on-state due to the self-heating effect caused by significant dissipated power, and the device then fails at the point (as denoted circle 2 or 3) where a snap-back occurs. All the snap-back points, e.g., circles 1, 2 and 3 in Fig. 1(a) define the loci in the low current regime of the I_b mode. At very high I_b levels, J_c decreases more rapidly with increasing V_c and exhibits a sudden drop or collapse before it goes into snap-back (see inset of Fig. 1(a)). The current collapse implies that the device has been in such an unstable condition that one emitter finger draws most of the current due to the thermal coupling [5]. Therefore, we refer the J_c collapsing points (as

denoted circles in the inset of Fig. 1(a) to the loci in the high current regime of the I_b mode. We found that the current collapse occurs only for large size devices, i.g., 2×3×40μm^2, and 2×3×50μm^2 indicating that the small size devices might not have significant "multi-finger effect" as typically found in other measurements [5] [2].

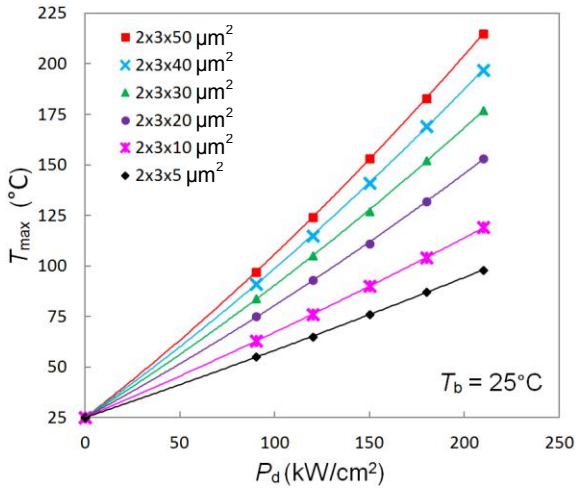

Fig. 5. Simulated peak temperature versus dissipated power density at room temperature for various device sizes (shown in the legend).

In Fig. 1(b), when V_b is low, the J_c keeps increasing with sweeping V_c due to the thermal effect [3] until the point where the snap-back occurs and therefore, those snap-back points, e.g., circles 1 and 2, define the loci in the low current regime of the V_b mode. When V_b is set higher, J_c increases initially at slow rate and then exhibits a steep jump to a high current regime where J_c peaks and goes down to the snap-back. This high current phenomenon is found in all size devices. It's also found that as soon as the J_c passes the peaks, the devices can easily fail even before the snap-back occurs. So we assign those peak points as denoted circles in the inset of Fig. 1(b) to the loci. To verify the aforementioned high current phenomenon for V_b mode, we calculate the IV curves as shown in Fig. 2 using analytical models which include most important physical mechanisms such as thermal, "Kirk", and breakdown effects [3]. Fig. 2 demonstrates that at high current regime, the J_c significantly increases to a peak point (as denoted circles in Fig. 2) and drops until the snapback. Detailed modeling will be reported separately.

Fig. 3 (a) and (b) show the measured SOAs with I_b mode and V_b mode respectively for all six emitter sizes. With increasing emitter size, the SOA shrinks. This size effect is attributed to the thermal resistance difference with size, which will be discussed in the next section. It is also noted that for the same device size, the I_b mode and V_b mode give rise to the significantly different SOAs. This is because the bias conditions at the base side are very different for the two modes. Specifically, for I_b mode, the base current is high and base voltage is low, but for V_b mode, the base voltage is high and base current is low. We can postulate that the two modes give rise to two extreme cases for the devices in real PAs.

THERMAL SIMULATION AND MEASUREMENT

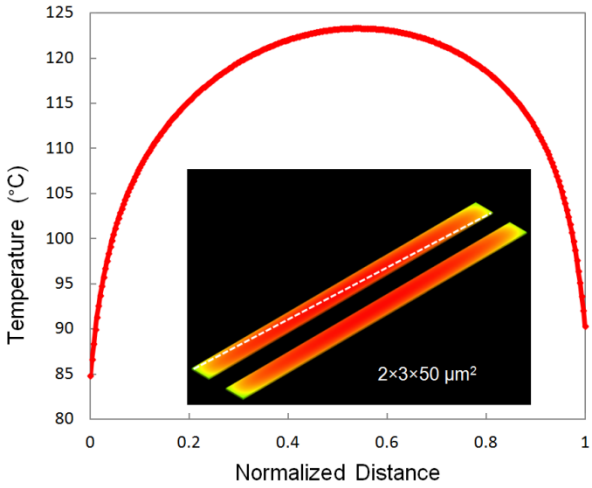

Fig. 6. Simulated temperature profile across one finger diagonally as indicated with a dash line in the inset which shows the temperature map of the two emitter fingers at the power density of 120kW/cm^2.

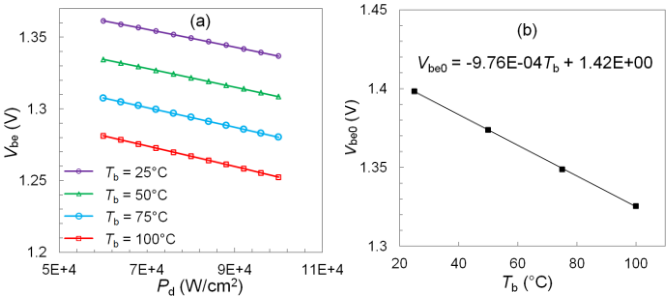

Fig. 7. (a): Measured base voltage (V_{be}) vs. dissipated power density (P_d) at different substrate temperatures, and (b): extrapolated V_{be0} vs. substrate temperature (T_b)

To obtain more precise results for the unit cells, a thermal simulation is performed at microscale level, which includes all detailed metal and dielectric layers, mesa geometry, and epi-layers. The tool CoventorWare [6] is used and the simulation is purely thermal without mechanical and electrical coupling. Fig. 4 shows a typical unit cell structure as measured in the SOA measurements. A cross section of the active device is also shown. The heat generation volume is defined under the emitter and vertically across the collector as indicated with the red dash line in Fig. 4, since the highest field is located within the collector [7]. The heat is assumed to be uniformly generated in the aforementioned volume. The substrate backside is set to a heat sink with constant temperature T_b. Fig. 5 shows the simulated peak temperature (T_{max}) in the unit cell versus dissipated power density (P_d W/cm^2) at room temperature for all different emitter sizes. Precisely speaking, the relation of the peak

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temperature and power density is parabolic, as we can see in Fig. 5. But empirically when the power is not too high, a linear relation is valid such as:

$$T_{\max} = T_{\mathrm{b}} + R_{\mathrm{th}} \cdot P_{\mathrm{d}} \qquad (1)$$

where R_{th} is the thermal resistance with unit of cm^2·°C/W. Fig. 5 clearly demonstrates that the thermal resistance increases with emitter size. It should be noted that the temperature is not uniform across the emitter area as shown in Fig. 6, and this non-uniformity becomes worse with increasing emitter area following the same size effect as the thermal resistance.

To compare with the simulation, we experimentally obtain R_{th} from thermal-electrical measurements. Basically the DC characteristics for each device size are measured at the substrate temperatures of 25, 50, 75 and 100°C. The DC measurement involves sweeping base current at various collector voltage V_{ce} while monitoring the collector current density J_{c} and base voltage V_{be}. We then obtain, for various V_{ce}, a group of curves of J_{c} vs V_{be}, from which the V_{be} versus dissipated power density $P_{\mathrm{d}} = (I_{\mathrm{c}} \times V_{\mathrm{ce}})/A_{\mathrm{e}}$ can be plotted for a specific J_{c}. The method detail can be found in [8] [9]. The relation of V_{be} and power density can be expressed as:

$$V_{\mathrm{be}} = \varphi \cdot R_{\mathrm{th}} \cdot P_{\mathrm{d}} + V_{\mathrm{be0}} \qquad (2)$$

where $\varphi = \frac{dV_{\mathrm{be0}}}{dT}$ is called thermal-electrical feedback coefficient which can be extracted by P_{d} = 0 from (2) with various base temperatures.

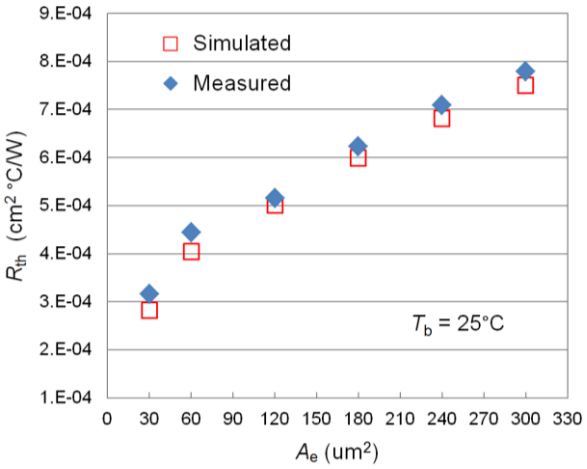

Fig. 8. Comparison between two thermal resistances for various emitter areas (A_{e}): one obtained by thermal simulation (solid diamond) and another one obtained by thermal-electrical measurement (hollow square).

As an example, Fig. 7 shows the measured V_{be} vs. dissipated power density for a current density of 40kA/cm^2 at different base temperatures (a) and the correspondingly extracted V_{be0} vs. T_{b} (b). From the linear line in Fig. 7(b), the thermal-electrical feedback coefficient of our InGaP/GaAs HBTs at a high current density of 40kA/cm^2 is obtained for the first time, which is about 0.98mV/°C.

From Fig. 7(a) and equation (2), we can obtain the thermal resistance R_{th} at room temperature and this value is then compared with the R_{th} obtained through thermal simulation for each device size as shown in Fig. 8. It's important to note that an average junction temperature in the simulation is used to compare with the measurement, because the temperature across the junction is not uniform as discussed previously and the result from the thermal-electrical measurement reflects an overall effect of the device junction. The comparison in Fig. 8 demonstrates that the device thermal resistances from the measurement and simulation are in good agreement for a large variation of device sizes. More importantly, the thermal resistance increases with increasing device size and this thermal size effect is consistent with the SOA size effect as discussed previously.

CONCLUSIONS

Both measurement and simulation have demonstrated that the SOA and thermal resistance of InGaP/GaAs HBTs follow the same size effect, revealing that the device thermal performance plays an important role in the SOA formation. The agreement between the theoretical analyses (thermal simulation and analytical modeling) and measurements indicate that the mechanism of SOA can be well understood.

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ACRONYMS

HBT: Heterojunction Bipolar Transistor

SOA: Safe Operating Area