SiN/Ge Lift-off: A Method for Patterning Films Deposited at High Temperature

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Abstract

In this work, we have developed a technique to circumvent the low-temperature limitations of conventional lift-off by using an inorganic bi-layer of silicon nitride (SiN) and Ge to replace conventional photoresist stacks. By using standard photolithography and anisotropic fluorine plasma etching, a lift-off profile was fabricated that has been exposed to temperatures as high as 670 °C with no failure in mechanical integrity. This paper documents the results from the initial proof-of-concept experiment and then shows the technique's application to patterning molecular-beam epitaxy (MBE) regrowth of n$^+$ GaN on GaN.

INTRODUCTION

Lift-off processing is a ubiquitous microfabrication technique that typically uses one or more patterned layers of photoresist to selectively place a thin film of metal (or dielectric [1]) on a sample surface. While photoresist-based lift-off has been a work-horse of the semiconductor industry for decades, it does have one key disadvantage that limits the versatility of the technique: conventional photoresists reflow at relatively low temperatures, typically between 100 – 150 °C. Since most dielectrics and semiconductors require deposition or growth temperatures greater than 300 °C to achieve high electrical and/or structural quality, photoresist is not a viable option for patterned lift-off of these materials.

The technique that is described in this paper uses conventional photolithography to transfer a pattern to an inorganic bi-layer of silicon nitride (SiN) and Ge. Ge has been used previously as a sacrificial/spacer layer in device processing [2] due to its selective dissolution in H_2O_2, and in this method serves as an undercutting layer that creates a SiN/Ge lift-off profile. Once the patterning photoresist is removed, the patterned SiN/Ge bi-layer allows for selective placement of one or more arbitrary films (metal, semiconductor, or insulator) on a substrate. The following sections will discuss the details of a proof-of-concept demonstration that illustrates the SiN/Ge lift-off process flow.

EXPERIMENTAL

In this experiment, a (100) GaAs wafer was used as the substrate for patterning. This choice allowed for sample cross-sections to be easily made via cleaving, prior to inspection in a scanning-electron microscope (SEM). The process began by depositing a 200 nm film of Ge by e-beam evaporation. Next, plasma-enhanced chemical vapor deposition (PECVD) was used to deposit 50 nm of SiN. After SiN deposition, standard contact photolithography was used to create openings in Microposit S1805 (Rohm and Haas) positive resist as shown in Figure 1. The feature size is nominally 1.7 µm.

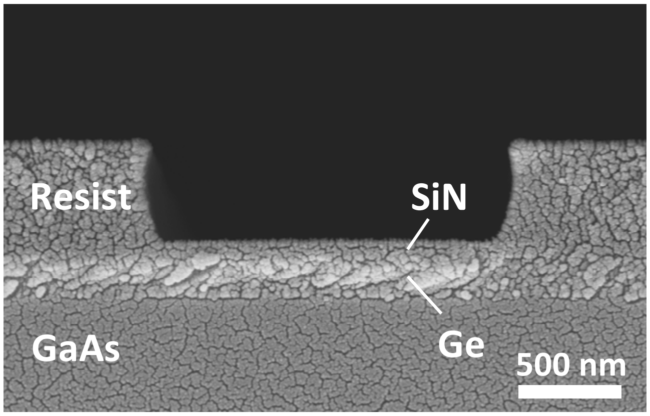

Figure 1 – SEM cross-section of evaporated Ge (200 nm) and PECVD SiN (50 nm) film layers on a GaAs substrate. S1805 resist was patterned using conventional lithography.

After development, the sample was then exposed to a 20 second, anisotropic SF_6 plasma etch in an inductively-coupled plasma (ICP) reactor. RF power to the ICP coil and bottom electrode were 200 W and 50 W, respectively. The chamber pressure during the etch was 5 mTorr. The resulting profile, in Figure 2 below, shows that the SF_6 plasma etches vertically through the SiN, and then isotropically into the Ge to create an undercut. For this etching time, the undercut length was 0.3 µm. After SF_6 etching was completed, the sample was then placed into an acetone bath to remove the patterning resist. Figure 3 shows a cross-section of the final SiN/Ge bi-layer feature.

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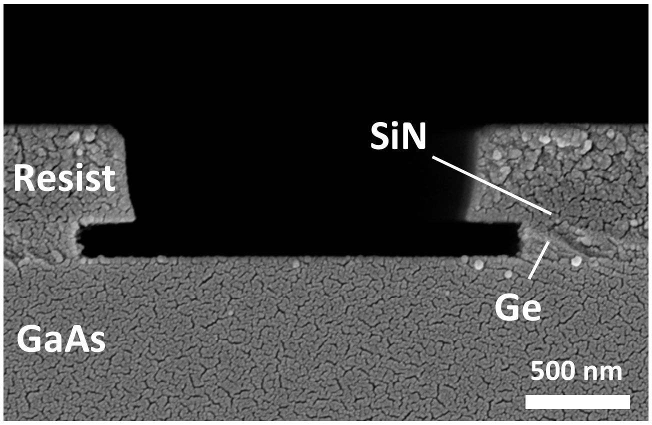

Figure 2 – SEM profile of feature after SF_6 ICP plasma etching to open SiN and etch Ge to create an undercut.

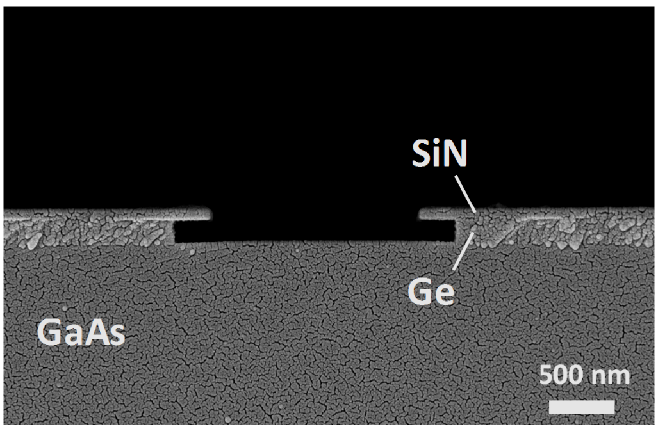

Figure 3 – SiN/Ge bi-layer profile after removal of resist with acetone.

To finally test the concept, we used the patterned SiN/Ge bi-layer to lift-off a thin film of metal. E-beam evaporation was used to deposit Ti/Au (20/80 nm) over the entire sample, resulting in the plan view micrograph shown in Figure 4. Lift-off was then carried out by submerging the sample in heated H_2O_2 (on a hot plate at 100 °C) for 150 minutes. During the lift-off, vigorous bubbling could be seen originating from feature openings as the H_2O_2 reacted with Ge. After lift-off of the SiN and overlying metal, the process was complete with the sample shown in Figure 5.

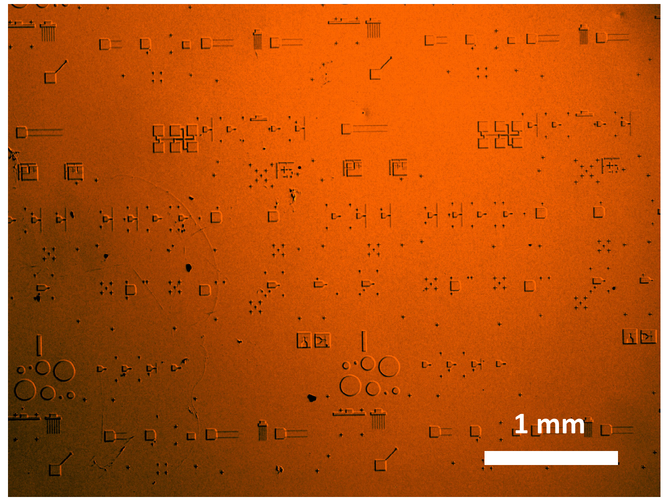

Figure 4 – Plan-view micrograph of SiN/Ge patterned sample after evaporation of Ti/Au (20/80 nm).

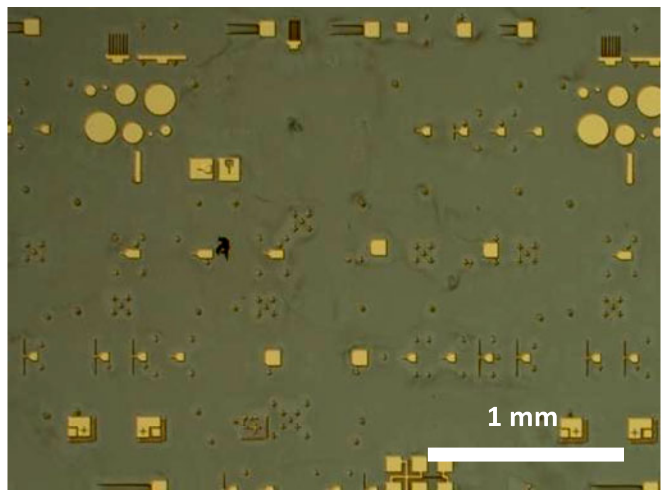

Figure 5 – Plan-view micrograph of Ti/Au patterned features after SiN/Ge lift-off in heated H_2O_2.

RESULTS AND DISCUSSION

In order to verify the thermal stability of patterned SiN/Ge features, a piece was cleaved from the sample in Figure 3 and was subjected to 5 minutes of annealing at 600 °C in N_2. The resulting cross-section, illustrated in Figure 6 below, shows no discernible change of the profile. While the melting point of Ge is 938 °C, the upper temperature limit of this technique depends on the specific substrate used, and whether it is thermodynamically stable with Ge.

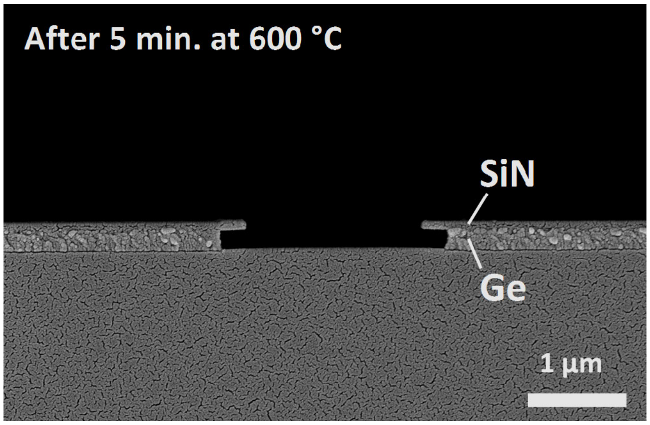

Figure 6 – SEM cross-section of a patterned SiN/Ge feature after 5 minutes of annealing at 600 °C in N_2.

To determine the relationship between SF_6 plasma etch time and Ge undercut length, several samples patterned with resist were exposed to different durations of etching. Figure 7 shows that the Ge undercut rate is controllable and self-limiting (likely due to the lateral diffusion length of excited F species.) On subsequent samples that used previously tested etch times, reproducibility of the undercut length was very consistent. This suggests that this process can be tuned to produce a precise and reliable amount of undercut. It should also be noted that if this process is to be used with large amounts of undercut (i.e. similar to 90 s etch sample in Figure 7), the thickness of the SiN layer should be increased above 50 nm to ensure mechanical integrity. Figure 8 shows that undercut length along a given patterned feature appears to have similar uniformity to a lift-off resist process.

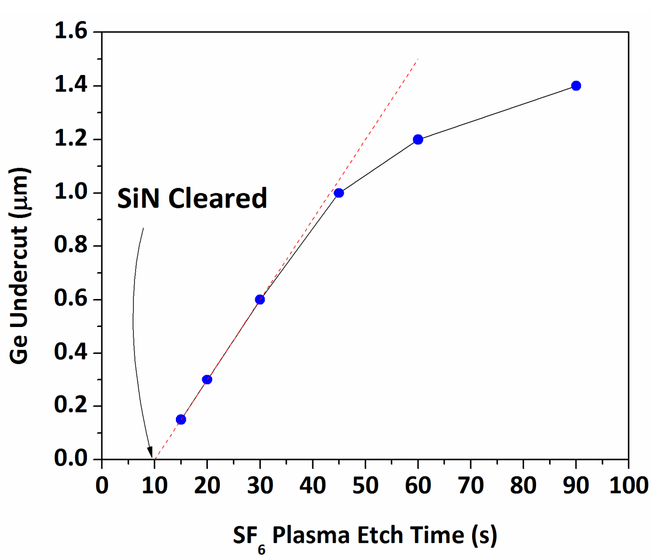

Figure 7 – Amount of Ge undercut versus SF_6 plasma etch time.

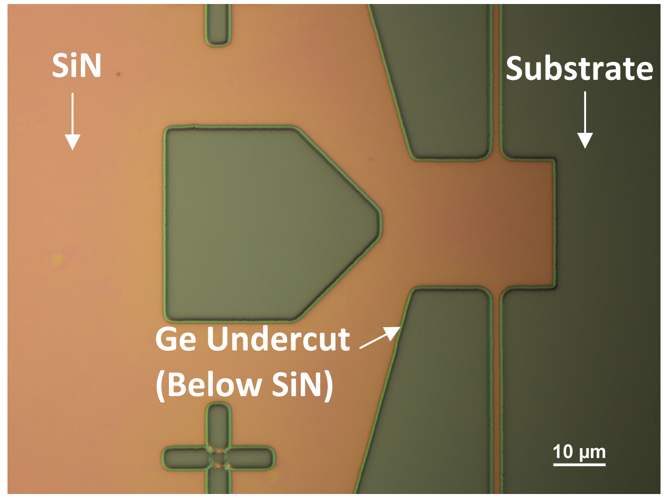

Figure 8 – Optical micrograph showing uniformity of nominally 0.5 µm Ge undercut around a device feature.

One disadvantage of this technique that was discovered during the proof-of-concept demonstration was that the lift-off time in heated H_2O_2 was longer than desired (150 minutes.) This had the unintended side-effect of causing pitting to occur in the GaAs substrate, which can be seen as faint discoloration around the metal features in Figure 5. One method to speed up the etch rate of Ge with H_2O_2 may be to alter the pH by adding KCl or KOH, which was previously observed to increase Ge etch rate in H_2O_2 by up to a factor of ten.[3]

An alternative to H_2O_2, which proved to be more time efficient, was to perform the lift-off in reactive XeF_2 gas. By using XeF_2, typically used for selective Si and Ge etching in micro-electro-mechanical systems (MEMS) processing, the entire SiN/Ge lift-off process is dry (in terms of not exposing the sample's surface to any wet-chemicals.) Also, since XeF_2 reacts with the Ge surface without the use of a plasma, Ge undercut is not self-limited by diffusion length of excited species.

To test out whether the SiN/Ge lift-off technique could be used to pattern epitaxial growth, we conducted an experiment using a plasma-assisted molecular-beam epitaxy (MBE) grown GaN on Si substrate. The starting GaN thickness was nominally 1 µm on (111) Si. After patterning with SiN/Ge (200/200 nm) features, the sample was loaded into the MBE. A 100 nm thick n^+-GaN layer was then grown at 670 °C. After cooldown, the sample was cleaved and examined in the SEM. Figure 9 shows that in the SiN/Ge openings, epitaxial GaN was regrown, while on top of the bi-layer, rough poly-crystalline GaN was deposited. At the feature edge of the SiN, a distinct tapering in the regrown GaN can be observed, which extends underneath the overhang. We suspect that this taper is caused by a shadowing effect, which is exaggerated by the incoming fluxes approaching the sample at off-normal incident angles.

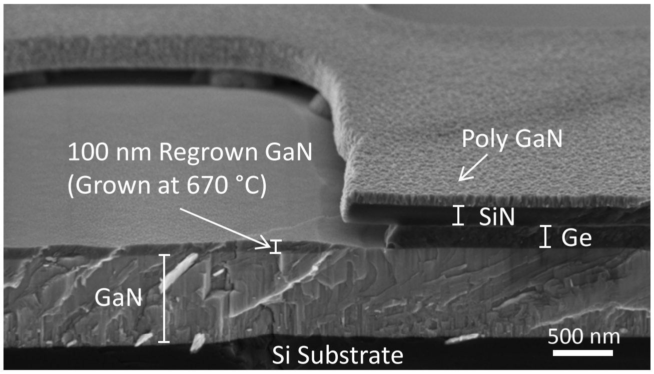

Figure 9 – SEM cross-section of SiN/Ge feature after MBE growth of 100 nm n^+ GaN performed at 670 °C.

After GaN deposition, the sample was placed into a XeF_2 exposure system. Ten 30 second long pulses of XeF_2 (P_{XeF2} = 4 Torr, P_{N2} = 35 Torr) were used to completely etch all of the Ge on the sample. During the process, the overlayers of SiN and poly-GaN cracked and partially were carried off the sample by gas flowing. Upon removal from the system, the sample was rinsed with deionized water and dried, which removed the remainder of the residual SiN/poly-GaN. Examination of the final sample in the SEM showed that the epitaxial n^+-GaN remained in place, in the desired pattern. This result is shown in Figure 10.

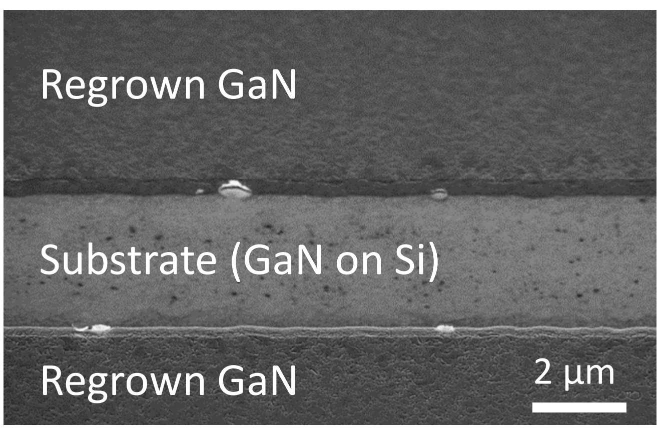

Figure 10 – Tilted SEM image of SiN/Ge patterned MBE regrowth of 100 nm n^+ GaN performed at 670 °C, after XeF_2 lift-off.

Conclusions

The results of this study show that SiN/Ge lift-off is an effective way to pattern arbitrary thin-films (metals, semiconductors, or insulators) that are deposited at temperatures above 150 °C. The versatility of this technique enables integration of multiple heterostructures and/or material systems onto the same wafer without the need for deep recess etching. Lift-off can be accomplished by either H_2O_2 solution or XeF_2 gas, depending on the surface sensitivity of the sample. For material systems such as the III-Sb family or N-polar GaN, this patterning technique prevents unintended surface etching by preventing exposure to basic photoresist developers. This technique was developed at the Naval Research Laboratory and has been submitted for U.S. patent consideration.[4]

Acknowledgements

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Acronyms

MBE: molecular-beam epitaxy
MEMS: micro-electro-mechanical systems
PECVD: plasma-enhanced chemical vapor deposition
SEM: scanning electron microscopy