

Improvement of LED Luminance Efficiency by Sapphire Nano PSS Etching

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Abstract

As a means of improving luminous efficiency of GaN-LEDs (Gallium Nitride - Light Emitting Diodes), pillar or cone shaped structures are periodically generated on sapphire substrates, which is called PSS (Patterned Sapphire Substrates). Using PSS, more light can be extracted (external luminous efficiency is increased) by a scattering effect (using micro-PSS with micrometer-size structures) or by a diffraction effect/photonic crystal effect (using nano-PSS with nanometer size structures). Also it has been reported that nano-PSS is more efficient than micro-PSS. [1]

The most effective way for the formation of nano-PSS is by dry etching using ICP-RIE (Inductively Coupled Plasma - Reactive Ion Etching) and employing photo resist (PR) as a mask. However, there have been challenges related to mask lithography and sapphire etching. In this research, the formation of nano-PSS by dry etching with a PR mask patterned using nano-imprint technology was studied.

First of all, to prevent deformation of the resist mask due to heat from plasma, the mask was UV-cured and hard-baked to increase its heat resistance, and it was confirmed that deformation didn't take place with processing carried out at 250°C. Secondly, to adjust the height of nano-PSS, etching parameters were studied and optimized. To adjust the height, selectivity against PR mask was crucial, and it was confirmed that selectivity can be controlled by adjusting bias RF Power, process pressure, and CHF₃ flow rate.

Lastly, to confirm the EL (electroluminescent) effect of nano-PSS, nano-PSS were fabricated on a sapphire substrates (height 100 – 750nm, spacing of 230nm) and the EL characteristics were compared, after GaN-LED structures were epitaxially grown. The EL intensity using nano-PSS (height 250nm) was 1.45 times stronger than without PSS formation.

INTRODUCTION

In order to improve luminous efficiency of GaN-LED structures epitaxially grown on sapphire, crystal quality improvement, internal quantum efficiency improvements through device structure changes, and external quantum efficiency improvements through light extraction

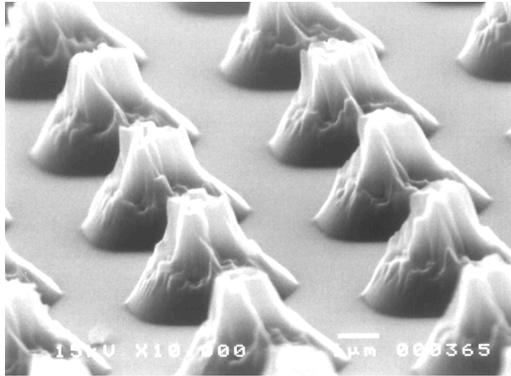
innovations, are required. To improve crystal quality, either a low-temperature GaN buffer layer to mitigate lattice mismatch, or ELO (Epitaxial Lateral Growth) can be effective. [2] Epitaxial structure improvement is effective for increasing the internal quantum efficiency, and to increase external quantum efficiency, light extraction improvement is effective by creating optical structures on the LED backside or sidewalls.

PSS is used for light reflection on the epitaxial layer/sapphire interface, by means of convex (or concave) patterning on sapphire substrates. This patterning aims to gather light towards the light extraction plane by scattering and diffraction of light on the bottom plane of the LED device, leading to improvement in the external luminous efficiency. Therefore, PSS is effective, not only for more efficient light extraction, but also for improvement of the GaN crystal quality.

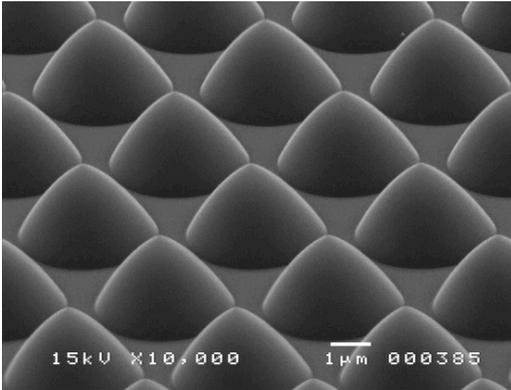
However, the sapphire substrate is very hard, chemically resistant, and is therefore very difficult to process. To form fine structures on the substrate, plasma dry etching is very effective, but it is accompanied by several problems such as a low etching rate and poor etch mask selectivity. A photo resist (PR) mask is used to pattern the sapphire substrate using ICP-RIE. Heat generated by the plasma will deform the PR, and the heat resistance of the PR mask has to be improved. Typically, the highest post-development process temperature for PR is around 120°C, but since high RF power is required for the etching of sapphire, heat from the plasma to the substrate increases, and the PR mask deforms (or burns) due to the increased substrate temperature as shown in Figure 1(a).

There are two ways to prevent this heat-induced problem: (i) directly cool the sapphire substrates to keep the PR mask below its deformation temperature; and, (ii) increase the maximum processing temperature of the PR mask. Direct cooling is carried out using mechanical or electrostatic clamping. Sapphire substrates for GaN-LED are mostly small wafers (3- or 4-inch), and a one-wafer-per-batch system will suffer from low throughput, while a

multiple-wafers-per-batch system with direct wafer cooling require a very complicated wafer clamping mechanism. In contrast, a multiple-wafer tray transfer system will have a simpler mechanism; but, without the ability of cooling each wafer, “PR burning” will result. [3]



(a) PSS fabricated using standard photo resist (PR); PSS etching without resist hardening



(b) PSS fabricated using resist hardening technology

Figure 1. Comparison of PSS formation with and without resist hardening.

Finally, mask lithography technology has to be improved to form nano-sized PSS (nano-PSS).

To solve these problems, a resist mask formed by using nano-imprint technology was introduced, procedures to increase the heat-resistant temperature of the resist was tested, and a study of selectivity control using ICP-RIE with a high density plasma source was carried out.

EXPERIMENTAL DETAILS

For the formation of etching masks, Novolak type photo resist was used. A stepper was used to expose the resist for micro-PSS formation, and nano-imprint technology was used for nano-PSS formation. In particular, imprint technology enables the formation of nano-size patterns over a wide area in a short period of time. A tray was used for wafer transfer, and the maximum processing temperature of

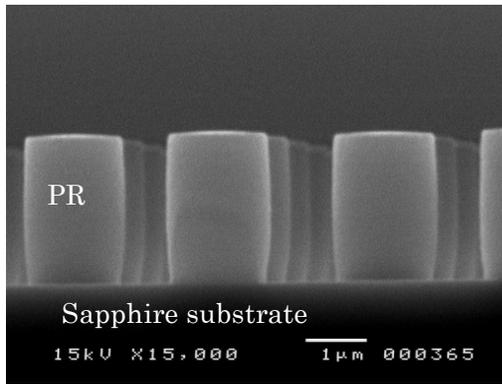
the PR mask, therefore had to be increased. To improve heat resistance, UV-curing by means of a UV lamp and hardening using a hot plate was carried out using micro-PSS patterns. The UV lamp was used for resist surface hardening, and a hot plate bake was used for the bulk hardening of the resist mask. In Figure 2, SEM pictures of PR masks are shown; (a) after lithography, (b) after UV cure, and (c) after hard bake. The SEM pictures show that the shape and size of the resist pattern remained the constant.

Figure 1(b) shows the result of micro-PSS etching using the hardened mask, and it was confirmed that smooth etching was observed without mask deformation. The same Novolak-type resist was used for a nano-PSS mask formed using imprint technology, and it also showed similar heat resistance since mask deformation was not observed.

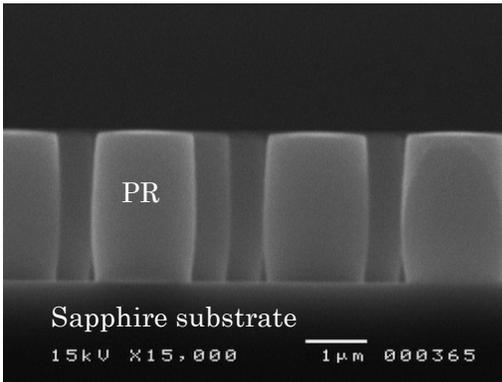
Sapphire etching was carried out using a SAMCO RIE-230iPC [4] with a Tornado ICP™ coil. A frequency of 13.56 MHz was used for both the ICP and Bias RF generators. Mixtures of Cl₂, BCl₃, Ar, and CHF₃ were used as the etchant gases. The lower electrode consisted of a water-cooled ESC (electrostatic chuck) and was maintained at room temperature. Profile, PSS height, and selectivity vs. the PR mask were measured while changing process parameters such as gas flow, process pressure, and RF power. GaN-LED structures were fabricated on the PSS substrates, and the light intensities for the various PSS patterns were compared.

RESULTS AND DISCUSSION

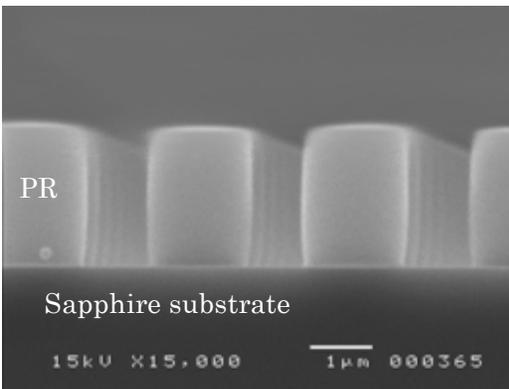
The periodic distance between adjacent nano-PSS patterns formed by imprint technology was designed to be 230nm, and the feature diameter was 145nm. The emission wavelength of the LED was 460nm, and the periodic distance mentioned above was half of the wavelength, and a photonic crystal effect by the nano-patterns was expected. A double layer of Novolak photo resist and silylated resist for UV imprint were formed on sapphire substrates. The nano pattern was imprinted on the top silylated resist layer. Resist residue after imprinting was removed using RIE with CHF₃ gas, and then, using the top layer as a mask, the lower Novolak resist was patterned using RIE with O₂. Later, a heat resistance process was carried out. In Figure 3, a SEM picture after RIE development is shown. Nano-PSS etching was carried out using the mask mentioned above. Figure 4 shows the relationships between the bias RF power, process pressure, and CHF₃ flow rate and the sapphire etching rate and sapphire/PR selectivity. As bias power was increased, the selectivity decreased, and this means that the change of PR mask etching rate is larger than that of sapphire, indicating that selectivity can be controlled with bias power.



(a) Process 1: After photolithography



(b) Process 2: UV-cured, at 120°C and at 1 atm for 10 minutes with nitrogen flow of 3 L/min



(c) Process 3: Hard-baked for 10 min at 250°C and 1 atm

Figure 2. Photo resist (PR) mask profile before and after resist hardening.

With bias powers over 150W, the resist mask was etched away, the sapphire substrate was over-etched, and therefore an accurate estimation of the selectivity and etch rate were not obtained. The bias power was set to 100W because selectivity decreased with increasing bias power. Selectivity increased with higher pressure, but the diameter of the pattern features increased because of deposition; therefore the best profile was obtained at a pressure of 0.3Pa. Also, selectivity was improved by increasing the CHF₃ flow rate. The optimized recipe was; 100W bias RF power, 0.3Pa

pressure, and 10 sccm CHF₃.

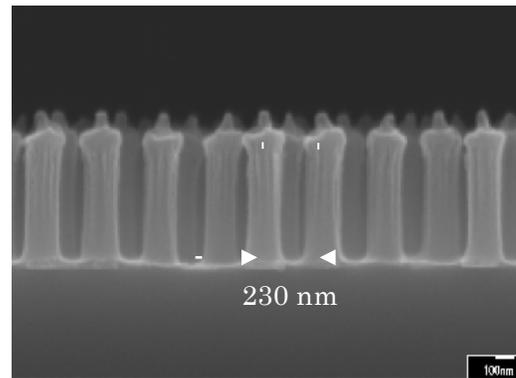


Figure 3. Photo resist pattern for nano-PSS after imprinting and RIE development.

Using the optimized recipe above, nano-PSS samples with heights of 100nm, 250nm, 500nm, 750nm were formed. Furthermore, GaN-LED structures were epitaxially grown, and before wafer dicing, the EL characteristics were measured. Figure 5 shows the comparison of the light intensity off different nano-PSS heights with the EL intensity for a sample without PSS. When nano-patterns formed on the sapphire substrate, the EL intensity increased with all the different heights. In particular, the EL intensity ratio hit its maximum at a height of 250nm and the normalized intensity ratio was 1.45.

It is known that dark spot density is independent of nano-PSS height and this indicates that the GaN crystal quality was not improved, but that the light extraction efficiency was improved due to a light diffraction effect or photonic crystal effect

CONCLUSIONS

It was confirmed that GaN-LED luminous efficiency was improved by forming nano-PSS on sapphire substrates using ICP-RIE. A PR mask patterned with nano imprinting was UV-cured for surface hardening and hard-baked for bulk hardening, and its heat resistance temperature was increased up to 250°C. This processing enabled the etching of sapphire wafers using a simple tray-transfer type ICP-RIE.

The relationship of each process parameter and the selectivity was confirmed for the purpose of nano-PSS height control, and data was obtained that showed that parameters such as bias RF bias power, process pressure, and CHF₃ flow contribute to the selectivity improvement.

Employing a nano-imprinted mask, resist hardening, and

using the optimized ICP-RIE recipe, nano-patterns were formed on sapphire substrates over a height range of 100-750nm, with a periodic distance of 230nm. Following the epitaxial growth of the GaN-LED structures on the PSS, the EL characteristics were measured. As a result, EL intensity using nano-PSS (height = 250nm) was found to be up to 1.45 times stronger than without PSS formation.

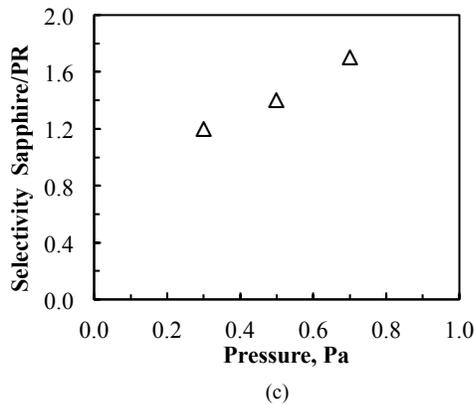
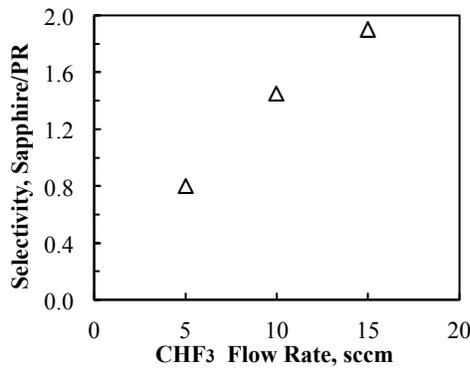
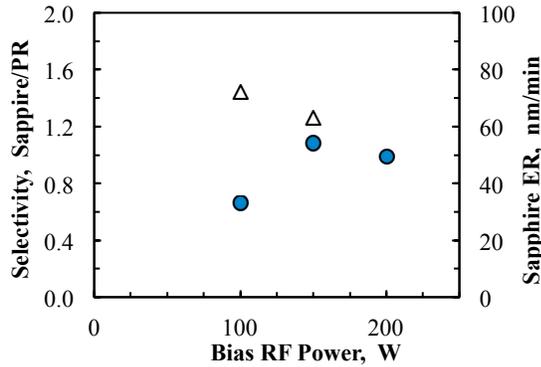


Figure 4. Relationship of etch parameters versus sapphire etching rate and photo resist selectivity: (a) selectivity and sapphire etch rate vs. bias power, (b) selectivity vs. CHF₃ flow rate, and (c) selectivity vs. process pressure.

Future challenges include optimizing the periodic distance of the pattern and pillar height, investigating their relationship to emission wavelength, and further

improvement of emission efficiency.

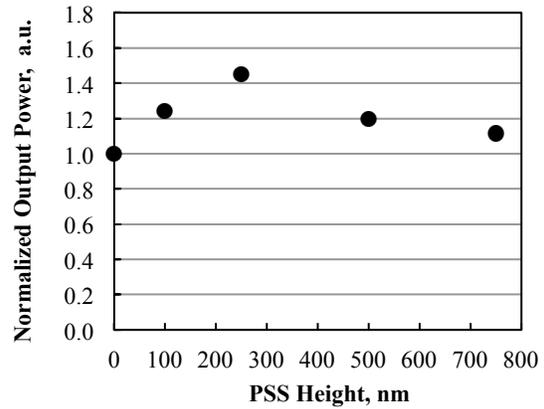


Figure 5. Height of nano-PSS formed using ICP-RIE vs. Electroluminescent (EL) intensity ratio. Non-PSS has a normalized output power of 1.0

Application of resist hardening technology to materials other than sapphire is being investigated. For example, it can be used for etching InP at high etching temperatures.

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REFERENCES

- [1] S. Miyoshi, R. Inomoto, N. Okada, K. Tadatomo, T. Nishimiya, M. Hiramoto and S. Motoyama: 11th APCPST & 25th SPSM, October 5, 2012, Kyoto University, Japan
- [2] K. Hoshino, N. Yanagita, M. Araki, and K. Tadatomo: Jpn. J. Appl. Phys., 40 L583, 2001
- [3] H. Ogiya, T. Nishimiya, M. Hiramoto, S. Motoyama and O. Tsuji: CS MANTECH Conference, April 23rd – 26th, 2012, Boston, Massachusetts, USA
- [4] H. Nakano, S. Nakagami, T. Nonaka and O. Tsuji: 7th APCPST & 17th SPSM, June 29 - July 2(2004), Fukuoka, Japan

ACRONYMS

- LED: Light Emitting Diode
- PSS: Patterned Sapphire Substrate
- EL: Electroluminescent
- PR: Photo Resist
- SEM: Scanning Electron Microscope
- ICP: Inductively Coupled Plasma
- RIE: Reactive Ion Etching