High-Voltage GaN-on-Silicon HEMT's

T. Boles[1], C. Varmazis[1], D. Carlson[1], L. Xia [1], D. Jin [1],
T. Palacios[2], G. W. Turner[3], R. J. Molnar[3]

[1] M/ACOM Technology Solutions, Lowell, MA
timothy.boles@macomtech.com; douglas.carlson@macomtech.com;
ling.xia@macomtech.com; donghyun.jin@macomtech.com; varmazis@comcast.net
[2] Massachusetts Institute of Technology, Cambridge, MA
tpalacios@mit.edu
[3] Massachusetts Institute of Technology, Lincoln Laboratory, Lexington, MA
turner@ll.mit.edu; rmolnar@ll.mit.edu

Keywords: GaN; GaN-on-Silicon; GaN HEMT's

Abstract

M/A-COM Technology Solutions has continued in the joint development efforts sponsored by the Department of Energy with MIT main campus and MIT Lincoln Labs to develop GaN-on-silicon three-terminal high-voltage/high-current HEMT switching devices. The first year developmental goals were for a three-terminal structure that has a reverse breakdown characteristic of >1200 volts and is capable of switching 10 amperes of current.

An average three-terminal breakdown of 1322 volts was achieved on a single finger 250 µm GaN-on-silicon HEMT device utilizing a source connected field plate with a 4.5 µm drain region overlap. An individual device breakdown on a single finger, 250 µm GaN-on-silicon HEMT device with a SCFP of >1630 volts was measured at a current of 250 µA (1 mA/mm) – One of the highest yet reported for GaN-on-silicon in the industry.

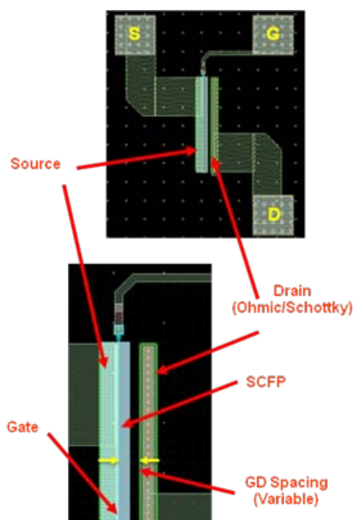

Fig. 1 – Details of Three-Terminal HEMT Devices Including Source Connected Field Plate Variants

INTRODUCTION

The following paper is a summary of the results to date of the developmental efforts at M/A-COM Technology Solutions of a Department of Energy sponsored joint effort in conjunction with MIT Lincoln Labs and the MIT Electrical Engineering and Computer Science Department to realize GaN-on-Silicon three-terminal HEMT devices having reverse breakdown voltages greater than 1200 volts.

With respect to three-terminal design structures to produce a GaN-on-silicon HEMT device having a >1200 gate–to–drain breakdown, the main approach focused on "normally on" device designs and was based upon M/A-COM Tech's standard high frequency test structures. The required high-voltage reverse breakdown was investigated by examining a range of larger source-to-drain spacings, and utilizing source connected field plate, SCFP, structures to spread the peak field in the gate-to-drain region.

DISCUSSION

A three-terminal test reticule, having single gate devices with 250 mm of gate periphery as well as multi-gate HEMT structures with 10 mm, 20 mm, and 30 mm gate peripheries was designed. The details of the single finger test FETs "Normally ON", depletion mode, three-terminal devices can best be visualized as shown in Figure 1. The specific dimensions are as summarized as follows: 1 µm gate length; 250 µm gate width; ohmic source and drain contacts; source connected field plate & non-field plate devices; multiple gate-to-drain spacings; and a 400 µm probe pad-to-probe pad pitch. The purpose of including multiple gate-to-drain spacings and SCFP overlap dimensions was to study and quantify the effect of these parameters on the overall HEMT breakdown.

The purpose of the field plate approach is to reduce the peak field at the drain side edge of the gate and spread the reduced field over the drain region of the HEMT structure. By reducing the peak field, higher voltages can be applied

10
a

Sponsored by Department of Energy under Contract Number DOE IA No.: DE-AI26-OE0000121
Award No. :DE-AI26-07NI43294/006

before the critical breakdown field strength is reached. The critical design features of this SCFP approach in terms of peak field modification are the overlap of the field plate onto the drain region and the thickness of the intervening dielectric

RESULTS

Measurements were made on-wafer for high-voltage, three-terminal, reverse breakdown characteristics on the single gate devices with ohmic source and drain contacts, standard non-recessed gates, and non-field plate devices having multiple GD spacings. In addition, single gate devices also having ohmic SD, standard non-recessed gates devices, and multiple GD spacings, but with source connected field plated devices also having multiple SCFP overlap dimensions were evaluated in this test matrix.

All measurements were made on these single finger HEMT devices having a gate width of 250 µm and a gate length of 1.0 µm with the gate pinched-off at a gate bias of -6.0 volts and at a drain current of 250 µA (1.0 mA/mm of gate periphery). Because of difficulties and voltage limitations with the auto tester, all high-voltage data was taken using a curve tracer. Due to the manual nature of the curve tracer measurements, the data was limited to 10 reticules.

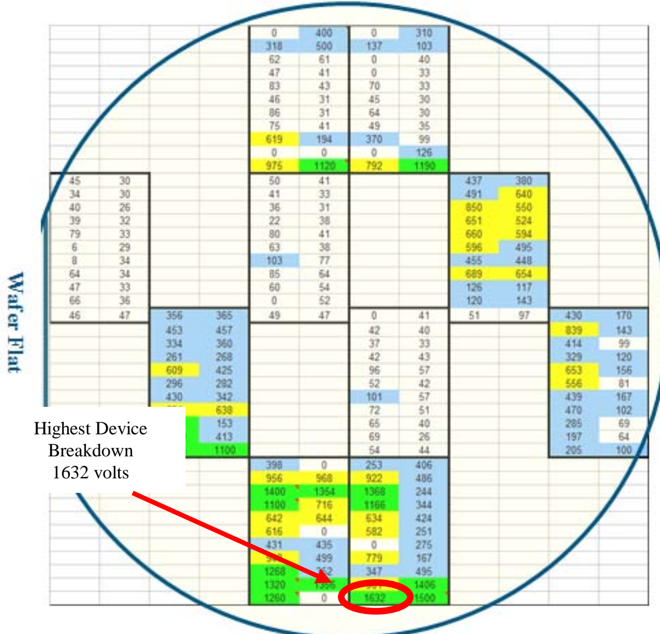

Fig. 2 – Wafer Map of Breakdown Voltages by Reticule Position

In Figure 2, a wafer map showing the range of three-terminal breakdown voltages that was observed on the various single finger FET geometries within each reticule is presented. A number of general characteristics can be seen. The center of the wafer seems to have lowest breakdown. In fact, the reticules with the highest breakdown are toward the edges of the wafer. As expected the devices with larger drain-to-gate spacings have higher reverse breakdowns. The highest individual device breakdown measurement occurred on a SCFP device with an extended source connected field plate drain overlap.

In order to make some comparisons between the various device topologies, the low breakdown reticules were excluded and an analysis of the remaining reticules was performed. The graphical results of this analysis are shown in Figure 3 and Figure 4.

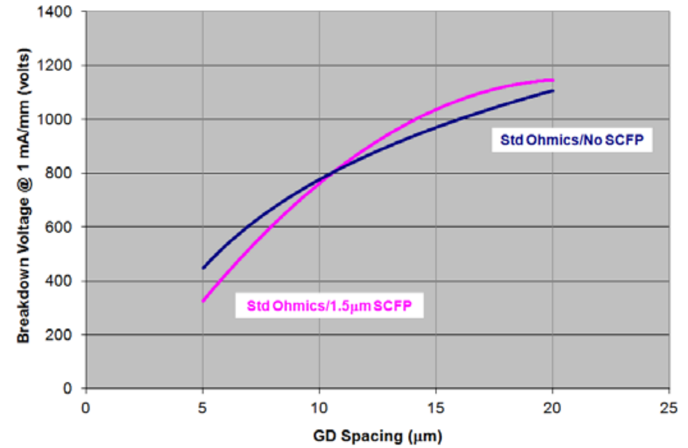

Fig. 3 – Breakdown Voltage as a Function of GD Spacing with 1.5µm SCFP and No SCFP

Figure 3 is a plot of the three-terminal reverse breakdown voltage as a function of gate-to-drain spacing with and without a source connected field plate and having standard ohmic contacts. The design purpose of the source connected field plate is to spread and reduce the peak field at the drain edge of the gate and allow higher voltages to be applied before critical field is reached enabling higher reverse breakdown.

As can be seen in Figure 3, as expected, larger gate-to-drain spacing results in higher reverse breakdown with a minimum average breakdown voltage of approximately 400 volts at a 5 µm gate-to-drain (GD) spacing and approximately 1200 volts at a 20 µm gate-to-drain (GD) dimension for the HEMT devices without a source connected field plate. This translates to a breakdown field strength in the drain region of 80 volts/µm ($8x10^5$ volts/cm) at a 5 µm GD spacing and at a 20 µm GD spacing the field strength begins to saturate but still has a very respectable value of 60 volts/µm ($6x10^5$ volts/cm). It is believed that the breakdown limitation for these non-field plated devices is due to the peak field at the drain-side edge of the gate exceeding the $3x10^6$ volts/cm theoretical limit of the AlGaN/GaN active layer structure.

Also in Figure 3, is a plot of the identical HEMT structures with the same gate-to-drain spacings but having a source connected field plate with a constant 1.5 µm field plate overlap beyond the gate edge toward the drain contact. It was expected that a significant increase in the breakdown characteristic would have been realized with the addition of the field plate structure to the basic HEMT topology. As can

be seen, this improvement was not realized and an essentially identical relationship of the three-terminal breakdown voltage versus the GD spacing was realized.

The observed lack of improvement in the breakdown voltage, as will be discussed further in the results presented in Figure 5, is believed to be due to the fact that a constant 1.5 µm overlap of the field plate over the extended drain region was employed. This 1.5 µm overlap dimension is felt to be insufficient to spread and moderate the peak field in the drain region resulting in build up to critical field and lower than expected breakdown.

In Figure 4, a plot of the a HEMT device having standard ohmic drain contacts and a fixed 20 µm gate-to-drain spacing as a function of a source connected field plate having a variable drain overlap dimension. In this case, it can be seen that the SCFP at larger drain overlap is certainly providing the expected boost in the device three-terminal reverse breakdown voltage.

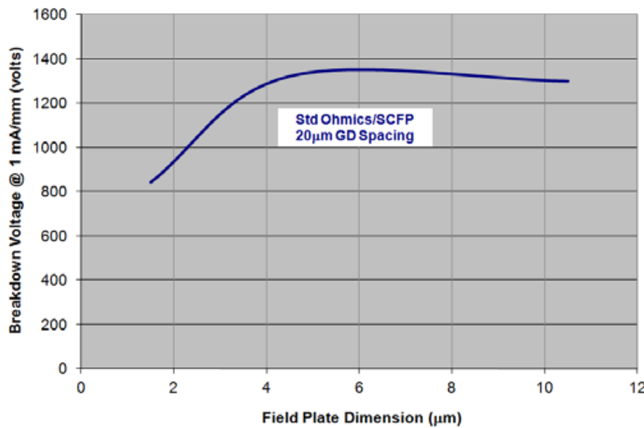

Fig. 4 – Breakdown Voltage as a Function of Drain SFCP Overlap for Standard Ohmic Contact HEMTs

It can be observed in Figure 4 that an increase of approximately 500 volts was achieved in the average breakdown voltage as the SCFP drain overlap was increased from 1.5 µm to 4.5 µm. The average breakdown value achieved at the 4.5 µm SCFP overlap dimension was 1322 volts. This translates to an average field strength in the drain region of 66 volts/µm ($6.6x10^5$ volts/cm). The highest breakdown voltage achieved on an individual device was measured at this 4.5 µm SCFP drain overlap spacing and was 1632 volts, corresponding to a drain field strength of 82 volts/µm ($8.2x10^5$ volts/cm). Lastly, in Figure 4, it can be seen that as the SCFP drain overlap dimension is further increased to 10.5 µm, there virtually no effect on the average three-terminal device breakdown voltage or drain field strength.

All of the above efforts concentrated on the high reverse breakdown blocking characteristics of the lateral AlGaN/GaN HEMT structures when in the OFF state, but it should be remembered that the three-terminal development goals also required the ability to handle 10 amperes of current from source to drain when biased in the ON state. In support of this requirement, the initial test matrix, included not only the single gate HEMT devices, which have been used to characterize the V_{ds} breakdown, but also a number of multi-gate HEMT designs having 10 mm, 20 mm, and 30 mm of gate periphery.

A standard device I_{max} measurement was used to characterize the current handling ability of these GaN HEMT structures. The I_{max} measurement is made by forward biasing the schottky gate electrode at a normalized gate current of 1.0 mA/mm (I_g = 1.0 mA/mm) of gate periphery at a range of V_{ds}. In the results presented in the following figures, an I_{max} for 10 mm devices was measured and is plotted over a range of drain bias voltages.

In Figure 5, the absolute I_{max} current of two 10 mm GaN HEMT devices having a 7 µm gate-to-drain spacing is plotted as a function of applied drain voltage. It can be seen that the transistor structure without a source connected field plate, SCFP, had a peak current handling capability of approximately 5.5 amperes at a drain bias of 7 volts. It can also be seen that as the drain voltage is increased, the I_{max} rolls off to value of 4.75 amperes at a V_{ds} of 15 volts. Since this is an on-wafer test at full wafer thickness and utilizing only a vacuum hold down for heat sinking, it is felt that this gradual current degradation is due to device heating as a result of approximately a peak power of 71.25 watts being dissipated in the GaN HEMT at the 15 volt drain bias

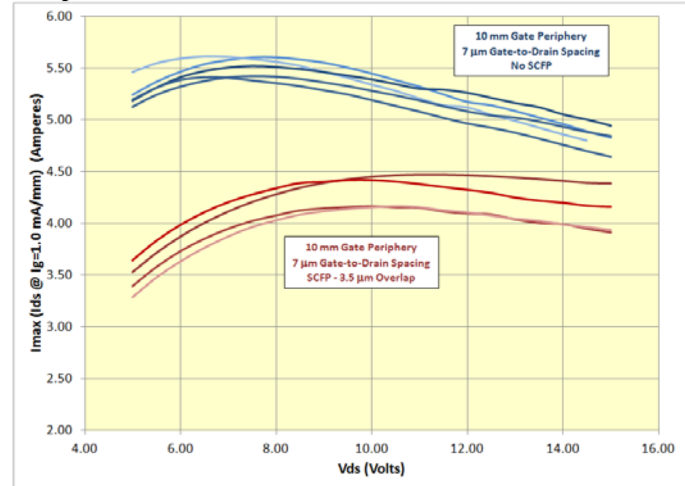

Fig. 5 – I_{max} vs V_{ds} for 10 mm Gate Periphery GaN HEMT Devices with 7 µm Gate-to-Drain Spacings

10
a

Also shown in Figure 5 is an I_{max} versus V_{ds} curve for a identical 10 mm HEMT except that a SCFP has been incorporated into the device structure. In this case, a slightly reduced I_{max} peak value of 4.25 amperes was observed over a 10 volt to 12 volt drain bias range with only a slight current degradation as the drain bias is increased to 15 volts. The source of the lower peak I_{max} current was confirmed to be an

increase in the device ON resistance, R_{on}, due to field spreading and a partial depletion of charge carriers in the gate-to-drain region directly under the SCFP drain overlap area in the HEMT structure.

In order to achieve the three-terminal 10 amperes peak current handling goal, several avenues need to be pursued. First, the thermal limitations observed in Figure 6, need to be addressed by thinning the wafers to a final thickness of 100 µm, depositing a gold back metallization, separating the wafer into individual die, and attaching the individual devices with a high thermal conductivity material, epoxy or solder, to a packaged heat sink. Second, the 1761 test matrix also includes 20 mm and 30 mm HEMT devices. These devices have yet to be characterized but simple linear scaling of the 10 mm devices would imply that the 20 mm device could achieve 8.5 amperes to 9.5 amperes of peak current handling and that the 30 mm structure would produce an I_{max} up to 13 amperes. Lastly, the multi-gate device layouts can be redesigned to further improve the thermal optimization by dividing the device into smaller active cells and spreading the dissipated power over a larger area.

CONCLUSION

A three-terminal evaluation mask was designed having a series of single finger HEMT structures to study the effect of SCFP plates, Schottky diode drain contacts, and gate recesses on the breakdown performance. Measured an average three-terminal breakdown of 1322 volts on a single finger 250 µm GaN-on-silicon HEMT device utilizing a source connected field plate with a 4.5 µm drain region overlap.

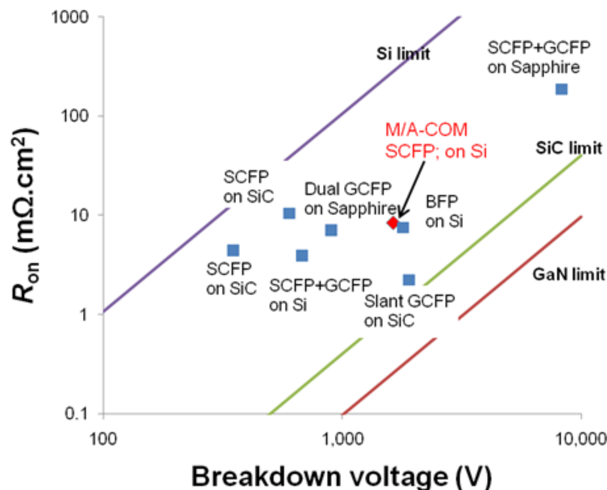

Fig. 6- MTS GaN HEMT - Comparison to Literature/Industry

Achieved an individual breakdown on a single finger 250 µm GaN-on-silicon HEMT device with a SCFP of >1630 volts at a current of 250 µA (1 mA/mm). An on-resistance of approximately 8 mΩ cm^2 of this single finger 1630 volt FET was measured and used to generate a plot of on-resistance versus breakdown voltage in order to compare against both material theoretical limits and various field plate geometries as presented in the literature. This plot is shown in Figure 6. It can be seen that the results compare extremely favourably with the reported state-of-the-art devices, regardless of substrate material or field plate approach.

Demonstrated over 5.5 amperes of I_{max} current utilizing a HEMT structure without a SCFP and having 10 mm of gate periphery, corresponding to a normalized current handling of at least 550 mA/mm. Also realized an I_{max} of 4.5 amperes and a normalized current density of 450 mA/mm on a identical transistor geometry but with the addition of a SCFP. No degradation in the device parameters was observed during the high-current characterization of either device structure. This is a measure of the survivability and ruggedness of this lateral GaN-on-silicon three-terminal HEMT design approach.

ACKNOWLEDGEMENT

The authors would like to acknowledge Mike Soboroff at the Department of Energy without whose support and funding none of this work would have been accomplished.

REFERENCES

[1] Timothy Boles, Costas Varmazis, Douglas Carlson, Tomas Palacios, “Effect of Isolation Techniques on GaN-on-silicon Breakdown Voltage”, International Workshop on Nitrides, September, 2010

[2] Y. F. Wu, A. Saxler, M. Moore, R. Smith, S. Sheppard, P. Chavarkar, T. Wisleder, U. Mishra, and P. Parikh, "30-W/mm GaN HEMTs by field plate optimization," *Electron Device Letters, IEEE,* vol. 25, pp. 117-119, 2004.

[3] W. Saito, Y. Takada, M. Kuraguchi, K. Tsuda, I. Omura, T. Ogura, and H. Ohashi, "High breakdown voltage AlGaN-GaN power-HEMT design and high-current density switching behavior," *Electron Devices, IEEE Transactions on,* vol. 50, pp. 2528-2531, 2003.

[4] W. Saito, Y. Kakiuchi, T. Nitta, Y. Saito, T. Noda, H. Fujimoto, A. Yoshioka, T. Ohno, and M. Yamaguchi, "Field-Plate Structure Dependence of Current Collapse Phenomena in High-Voltage GaN-HEMTs," *Electron Device Letters, IEEE,* vol. 31, pp. 659-661, 2010.

[5] X. Huili, Y. Dora, A. Chini, S. Heikman, S. Keller, and U. K. Mishra, "High breakdown voltage AlGaN-GaN HEMTs achieved by multiple field plates," *Electron Device Letters, IEEE,* vol. 25, pp. 161-163, 2004.

[6] N. Ikeda, S. Kaya, L. Jiang, Y. Sato, S. Kato, and S. Yoshida, "High power AlGaN/GaN HFET with a high breakdown voltage of over 1.8 kV on 4 inch Si substrates and the suppression of current collapse," in *Power Semiconductor Devices and IC's, 2008. ISPSD '08. 20th International Symposium on*, 2008, pp. 287-290.

[7] Y. Dora, A. Chakraborty, L. McCarthy, S. Keller, S. P. DenBaars, and U. K. Mishra, "High Breakdown Voltage Achieved on AlGaN/GaN HEMTs With Integrated Slant Field Plates," *Electron Device Letters, IEEE,* vol. 27, pp. 713-715, 2006.

[8] Y. Uemoto, D. Shibata, M. Yanagihara, H. Ishida, H. Matsuo, S. Nagai, N. Batta, L. Ming, T. Ueda, T. Tanaka, and D. Ueda, "8300V Blocking Voltage AlGaN/GaN Power HFET with Thick Poly-AlN Passivation," in *Electron Devices Meeting, 2007. IEDM 2007. IEEE International*, 2007, pp. 861-864.