Layout Practices for Die Size Reduction on InGaP/GaAs HBT MMICs for Handset Power Amplifier Applications

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Abstract

InGaP/GaAs HBT has been widely used in power amplifier (PA) design for wireless communications due to its high linearity and high efficiency. The latest mobile devices, which offer the user mobile Internet and other multimedia services on the move, draw on far more data than previous generations of mobile phones. The number of power amplifiers in the smartphone is increased to cover GSM, UMTS and LTE applications with varieties of frequency bands for global roaming. The PA module size and cost are other important aspects of products beyond performance. This work presents a 30% MMIC die size reduction from several changes in layout approaches.

INTRODUCTION

The growth of mobile internet and multimedia services has been explosive in recent years [1]. These mobile devices are required to support higher data rates promised by 3G WCDMA/HSPA, and even 4G LTE standards, with backward compatibility to the legacy 2G GSM and 2.5G GPRS/EDGE standards. In the meantime, a combination of frequency bands will need to be supported. It means plenty of PAs are required in the smartphone or tablet. How to reduce the cost and size of FEM is an essential topic for commercial mobile products [2]. Therefore, advanced packaging technique and/or die size reduction of MMICs plays a key role in module size shrinkage and cost reduction.

This paper will demonstrate improved layout practices for die size reduction on InGaP/GaAs HBT MMICs. Several approaches producing shrinkage for unit cells, power cells, and dicing streets are discussed.

DEVICE FABRICATION AND FEATURES

This work was done by WIN's 4th generation InGaP/GaAs HBT process [3,4]. The 4th generation HBT process, so called HBT4, included two interconnection metal layers (M1 and M2) and a thicker SiN layer as the dielectric layer between M1 and M2. A thicker SiN film instead of using

Polyimide as dielectric film can provide better mechanical and moisture protection. The thickness of the two metal interconnection layers are 1um evaporated and 4 um plated Au for M1 and M2, respectively. MIM capacitors with unit capacitance of 570 pF/mm^2, stacked MIM capacitors with unit capacitance of 870 pF/mm^2, and thin film resistors with sheet resistance of 50 Ohm/sq are also featured.

UNIT CELL DESIGN

In order to shrink the die size for multimode multiband (MMMB) PA, more flexible HBT design is presented in this work. Table 1 shows two kinds of HBT unit transistors with both horizontal and vertical orientations of emitter fingers. Vertical orientation means that the emitter finger is along the crystal direction (011), and horizontal orientation is perpendicular to the vertical one. As Fig. 1 shows, two orientations of HBTs can be implemented in a multi-band PA for realizing two power stages for high band and low band in a single die more easily and die size efficiently.

Table 1
Illustration of horizontal and vertical orientation HBTs

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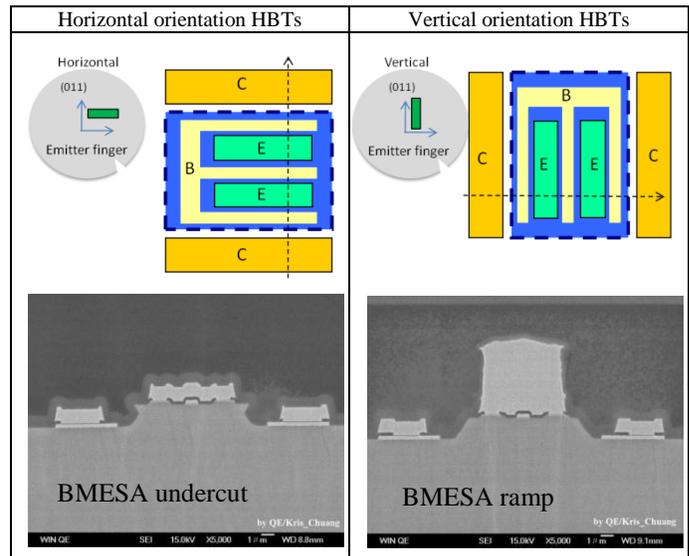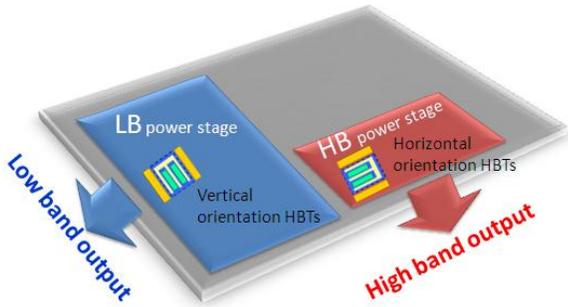
Fig. 1 Illustration of both horizontal and vertical orientation HBTs applying to Multi-Band PA.

As Fig. 2 shows, Gummel plots and I-V curves of vertical and horizontal orientations HBTs overlap very well.
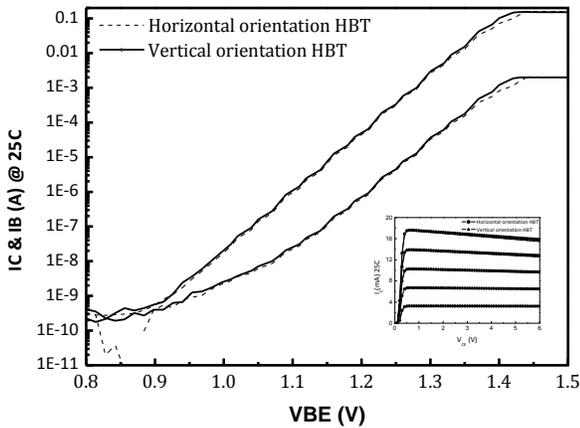

Fig. 2 Comparison of Gummel Plot and I-V measurements between horizontal and vertical orientation HBTs. The DC characteristics between horizontal and vertical orientation HBTs are identical.

Besides two orientations of emitter finger, this work demonstrated two configurations of HBT unit transistor. As Table 2 shows, Type-A HBTs are the conventional layout which has a base metal finger surrounds emitter mesas to form the B-E-B-E-B structures. In order to improve the power gain of unit HBT transistors, Type-B HBTs were proposed. Compared to conventional Type-A HBTs, Type-B HBTs which was E-B-E structure, removes the outer base metal fingers to reduce the base-collector capacitance (Cbc) by shrinking the base mesa area and further enhances the power gain.

Fig. 3 shows the comparison results of maximum available gain (MAG) between Type-A and Type-B HBTs. Type-B HBTs show higher MAG than Type-A HBTs due to the lower Cbc capacitance. Therefore, Type-B HBTs can provide around 1 dB higher power gain for frequencies below 3 GHz for cellular power amplifier applications.

Table 2
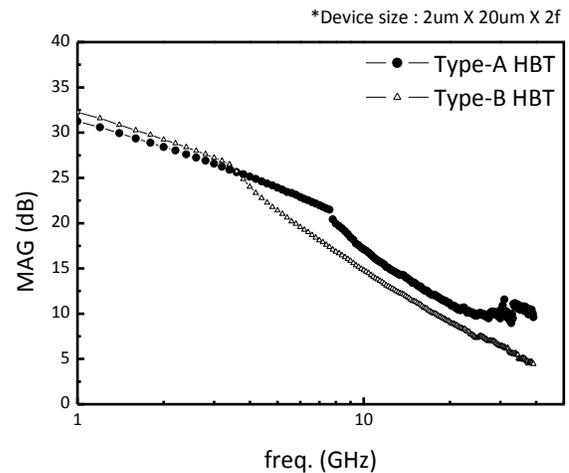The illustration of Type-A and Type-B HBTs

Fig. 3 Maximum Available Gain (MAG) between Type-A and Type-B HBTs. Type-B HBTs show higher MAG than Type-A HBTs.

EMITTER AREA SHRINKAGE

Cellular PAs are typically operated class-AB for lower DC power consumption and higher efficiency. The quiescent current (Icq) of the transistors in class-AB is typically biased at a relatively lower current density. Reducing the emitter area properly is the way to utilize the emitter active region more efficiently. A typical unit transistor configuration composed of 3 fingers * 40 um long * 3 um wide (E403) was experimented with to reduce its emitter area to achieve better performance. The smaller device consisted of 3 fingers * 28 um * 3 um (E283), and is proposed to demonstrate superior performance than E403. As Fig. 4 shows, E283 achieves higher gain under any current density due to the smaller BC junction capacitance.
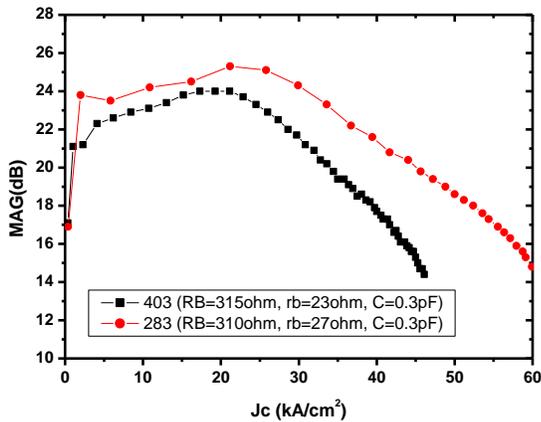
Fig. 4 Maximum Available Gain (MAG) between unit cell E403 and unit cell E283. The latter shows higher MAG.

Fig. 5 shows the comparative results of the power performance at 0.9 GHz between E403 and E283. DUTs are attached on an evaluation board with impedance matching. Power cell-A is composed of 32 cells of E403, with a total emitter area of 11520 um^2. Power cell-B is composed of 32 cells of E283, with total emitter area of 8064 um^2 – a 30% emitter area reduction. Both power cell-A and cell-B are biased at the same quiescent current 200 mA under VCE of 3.6 V. Power cell-B with smaller emitter area demonstrates higher gain and efficiency, and delivers the same saturated output power as power cell-A.
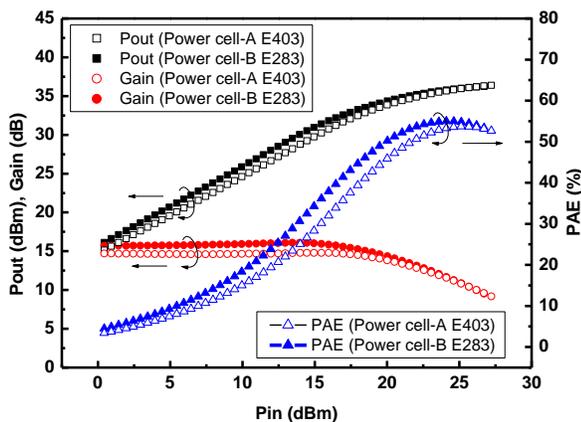

Fig. 5 A comparison of power performance between power cells built with unit cell E403 and unit cell E283.

Table 3 shows the detailed power performance comparison. Power cell-B shows 1 dB higher linear gain and around 1 % PAE enhancement. The P1dB and saturation power of power cell-B is around 34 dBm and 36 dBm. Respectively, which is almost identical to power cell-A. Therefore, power cell-B with a smaller emitter area unit cell can deliver the same output power with higher gain and better efficiency.

Table 3
Ruggedness test results

Cell Name	Emitter Area (um²)	Gain (dB)	P1dB (dBm)	PAE@ P1dB (%)	Psat@ Pin=26.5dBm (dBm)	PAE max (%)
Power cell-A	11520	14.7	34.13	48.9	36.24	55.0
Power cell-B	8064	15.7	34.09	47.2	36.30	53.7

The ruggedness performance will be one of the concerns when the device is operating at higher power density - delivering the same output power with smaller emitter area. Table 4 shows the results of ruggedness tests for power cell-A and cell-B. VSWR's of 10:1, 20:1, and 50:1 for 360 degree all phase rotation were tested under an output power of 35 dBm. Devices are biased at 3.6V and 5V. The output power will be checked before and after all phase VSWR swing. Less 10% power degradation after ruggedness test is the criterion of passing ruggedness test. Both power cell-A and cell-B can pass all conditions of ruggedness test. According to the ruggedness test results, power cell-B under higher power density can demonstrate the same ruggedness as power cell-A. Therefore power cell-B not only shows superior performance to power cell-A, but also demonstrates the same robustness under high impedance mismatch.

Table 4
Ruggedness test results

Device	Total area	VCE	Pout	VSWR		
				10:1	20:1	50:1
Power cell-A	11520 um²	3.6V	35 dBm	Pass	Pass	Pass
		5V		Pass	Pass	Pass
Power cell-B	8064um²	3.6V		Pass	Pass	Pass
		5V		Pass	Pass	Pass

PROCESS IMPROVEMENT FOR COMPACT MMIC DESIGN

Besides flexible unit cell design, more compact dicing street structures and smaller through-wafer vias can be achieved by using WIN's 4th generation InGaP/GaAs HBT process. Fig. 6 illustrates that the circuit-to-circuit spacing is dominated by the dicing street structure and opening width. Dicing street opening width can be reduced by implementing laser dicing instead of sawing process. Moreover, a compact dicing street structure with the spacing between any pattern in the MMIC and the street edge smaller can be achieved by using a pure SiN dicing street structure.

A smaller through-wafer via is also presented in this work. The diameter of the via is reduced from 40 um to 30 um. As Fig.7 shows, the power cell area can be shrunk by implementing the power cell-B, flexible HBT unit cell, and the smaller via diameter. The overall MMIC design can be

10 b

reduced 30% by the smaller power stage area and compact dicing street. Table 6 indicates that the total die size is shrunk from 0.92 mm^2 to 0.65 mm^2.
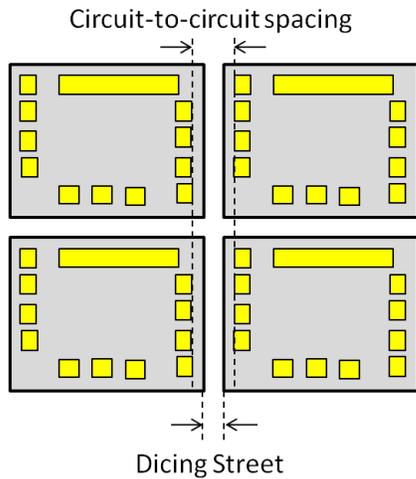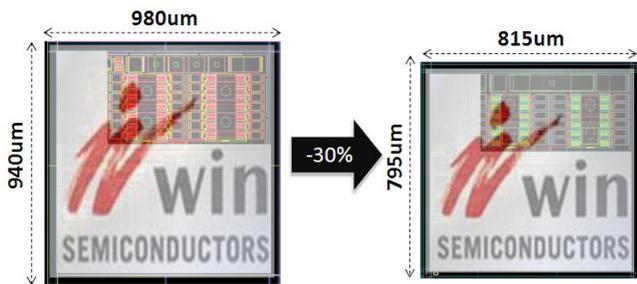

Fig. 6 Dicing street structure

Fig. 7 Die size reduction.

Table 6
Comparison of MMIC areas

Device	Width	Length	Total area
MMIC-A	980 um	940 um	0.92 mm^2
MMIC-B	815 um	795 um	0.65 mm^2

CONCLUSIONS

In conclusion, this paper has demonstrated a 30% die size reduction of an InGaP/GaAs HBT MMIC with better power performance and identical ruggedness performance. The die size reduction was achieved by flexible HBT layout design, proper selection of device size, and compact layout design rules.

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ACRONYMS

HBT: Heterojunction Bipolar Transistor
MMMB: Multimode Multiband
BMESA: Base Mesa
VSWR: Voltage Standing Wave Ratio