

Evaluation of Material and Process Contributions to BiFET Variation Using Design of Experiments

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Abstract

In this paper we present a method to separate the impact of feature size variation and material/gate etch variation in field effect transistors (FETs) manufactured in our BiFET process. The key to this separation is the realization that material and gate etch variation move the I_{dss} (zero bias drain current) and threshold voltage (V_p) along a line determined by I_{dss} vs. V_p^2 while feature size variations break this correlation and move the I_{dss}/V_p perpendicular to this line. This method of separation should also be applicable to understanding HEMT devices that use a power-recess.

INTRODUCTION

The understanding of FET variation is important for circuit design, modeling, and process monitoring. Most manufacturing facilities track saturation current (I_{dss}) and pinch-off voltage (V_p) for FETs, but these parameters are usually considered independent entities. For FETs, it is difficult to decouple the parameter variation due to starting material from process induced changes. We show that by exploiting the known relationship between I_{dss} and V_p , we can partially decouple material induced changes and fabrication induced changes. Using a design of experiment approach we show that material and gate etch move the

I_{dss}/V_p^2 points along a line while variation in FET geometries, (channel width, gate width, and gate length) causes points to deviate from this line. We also observe interactions among these factors that can cancel or enhance the deviation from the ideal line. This shows that looking at the correlation of these parameters, rather than just the parameters themselves, is useful for better understanding and process control.

DESCRIPTION OF EXPERIMENTS AND ANALYSIS

During the modeling and characterization of FETs in our BiFET process [1], we performed a number of experiments to explore process variation of the FET parameters, in particular I_{dss} and V_p . These included various experiments on material parameters (DOE1, DOE4, and DOE5) where the channel doping and thickness were varied, DOE2 where the etch-stop and growth conditions were varied, and DOE3 where the base, emitter, and doping layer above the emitter but under the channel (buffer) were modified. Other experiments we analyzed included different etch tools, different gate metallization, forming the gate at different steps in the process, and varying many of the material parameters and growth conditions. We observed that plotting the means of I_{dss} vs. V_p^2 for all of these experiments all on approximately the same line, shown in Figure 1, where V_p is (defined as the voltage at which $I_d=2.5\% I_{dss}$ is obtained).

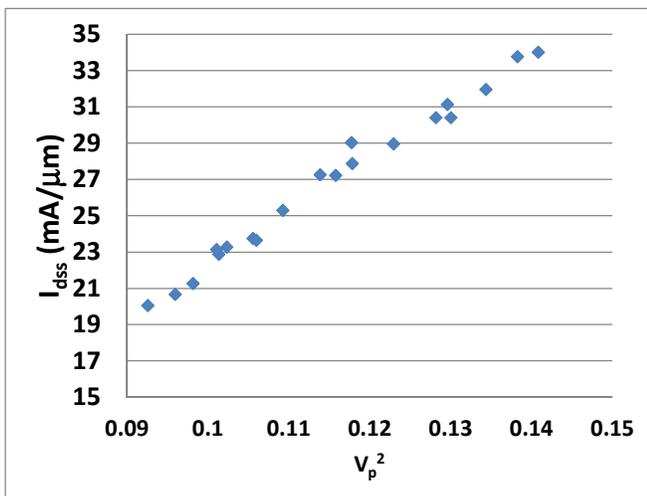


Fig. 1 Plot of mean data from process and material growth splits.

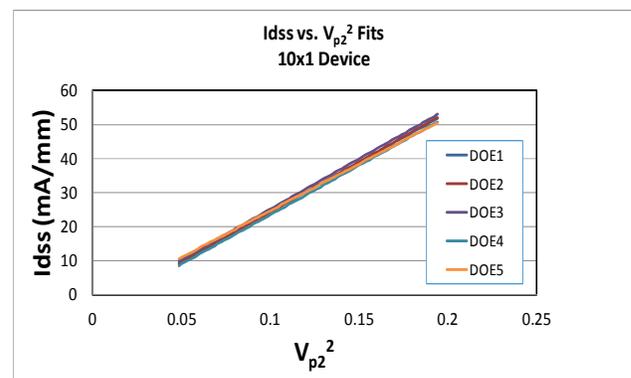
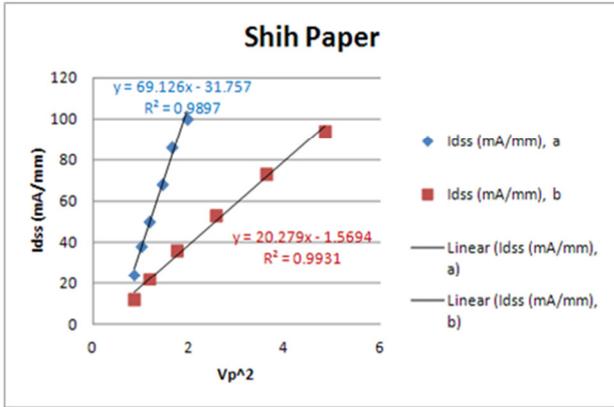
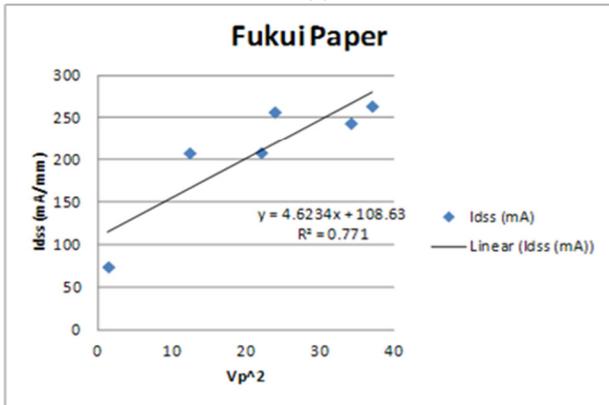


Fig. 2 Resulting Linear Fit from Various Material Designs of Experiment (DOEs)

10
b



(a)



(b)

Fig. 3. I_{dss} vs. V_p^2 for examples from literature. (a) is from [4] and series a is for a power device while the b series is for a low noise device. Gaussian doping profiles and simulated gate etch depth variation. Fig 2 (b) is from [5] where doping (N), active channel thickness (a), gate length (L), gate width (Z).

The variation of I_{dss} along this line is readily included in compact models for circuit simulation [2]. The rationale for using the square of the pinch-off is following [3] and re-writing as:

$$I_{dss} = k \left(\frac{W + dW}{L + dL} \right) V_T^2 \quad (1)$$

and since V_T and V_p are correlated, we further approximate this as, and re-arrange, to get:

$$\frac{I_{dss}}{V_p^2} = k \left(\frac{W + dW}{L + dL} \right) \quad (2)$$

Where dW and dL are changes in the gate width (W) and length (L), respectively. k is a constant (for a given technology). From our interpretation of this data, the k constant depends on both material and gate-etch (gate thickness) parameters). The second term (in brackets) should depend on process induced layout changes. From the

TABLE I
DESCRIPTION OF DOE STATES FOR EXPERIMENT

Run	Gate Width (Wg)	Channel Width (CH)	Gate Length (L)	Point (x 3σ)
1	--	--	0	-2_-2_0
2	-	-	0	-1_-1_0
3	--	++	0	-2_+2_0
4	-	+	0	-1_+1_0
5	++	--	0	+2_-2_0
6	+	-	0	+1_-1+0
7	++	++	0	+2_+2_0
8	0	0	0	0_0_0
9	0	-	-	0_-1_-1
10	0	+	-	0_+1_-1
11	0	-	+	0_-1_+1
12	0	+	+	0_+1_+1

observation of Fig. 1, we then plotting and fit data for a subset of these experiments, shown in Fig. 2, that led to the observation that material and gate formation changes only shifted data along this line, not perpendicular to it. To verify that this behavior was not unique to our BiFET process, we examined the behavior of I_{dss} - V_p^2 from [4] and [5] as shown in Figure 3. [4] Shows that, as a result of gate etch variation, there will be a linear relationship of I_{dss} vs. V_p^2 . The plot of reference [5] data also confirmed the trend of I_{dss} vs. V_p^2 . This shows that our observations are more generally applicable.

Over large volumes of data, there are points that deviate from this line, primarily because of the bracketed term in Eqn. (2). The broadening of the data along this line (so that the data different from the expected behavior) is not currently accounted for in models and cannot be observed if only I_{dss} is monitored. To explore the causes of this (which is normally assumed to due to gate length variations), we laid out an experiment where we varied the FET layout by DOE (gate length, gate width, and channel width – shown in Fig. 4 and defined in Table 1) and measured key FET performance parameters. The reason for selecting these particular factors they are the most likely – besides material

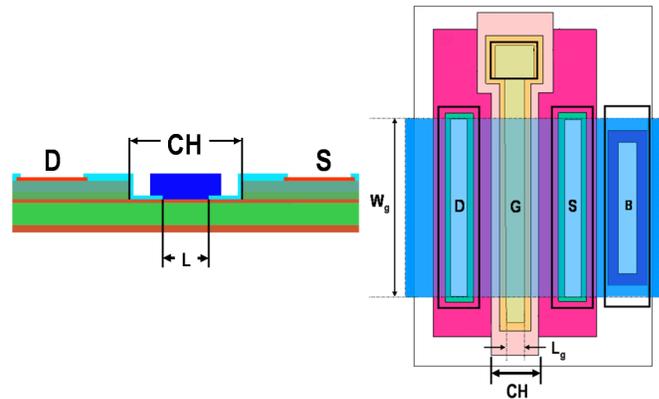


Fig. 4. Schematic cross-section showing parameters used in Table I.

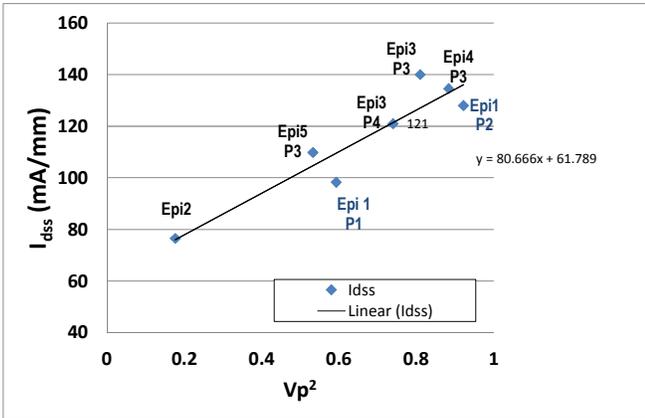


Fig. 7. Comparison of the distance method applied to our layout DOE, gate formation tools, material growth DOE, and gate etch tool.

To show the applicability to HEMT processes, we plotted mean values of $I_{dss}-V_p^2$ for several different processes (indicated by P#) generations in Fig. 7. The main variation in the materials is the Schottky layer on which the gate is placed (indicated by the label Epi#). The same general behavior is observed as for the BiFET. The gate length is longer on the processes labeled Epi1 and they fall below the line as expected. Re-plotting this data as distance in Fig. 8, we can infer that there are other process differences that account for the deviation from the line. In particular, the recess to gate metal spacing is different as are the gate lengths. This highlights the possibility of using a similar experiment to understand the correlation of I_{dss} and V_p^2 for HEMTs as well.

CONCLUSIONS

We first showed that for variations in a given FET process, a plot of I_{dss} vs. V_p^2 should follow a straight line. This was verified comparing simulation and measured data from literature. We showed that this results in material or gate formation differences shift the (I_{dss}, V_p^2) point along a diagonal determined by a linear fit of I_{dss} vs. V_p^2 while variations FET lateral dimensions move the (I_{dss}, V_p^2) orthogonal to this line. To understand what layout factors caused non-ideal behavior, we performed a DOE based experiment using layout factors. To easily highlight and compare the influence of these factors, we used the distance of these points to the expected line. The interaction of these factors was also shown to be important. Finally, we used the distance method to compare material, process, and our layout DOE. Applying this method to available data on pHEMT processes also showed it can be used to evaluate if the layout variation or material/gate formation caused the deviation from the expected behavior.

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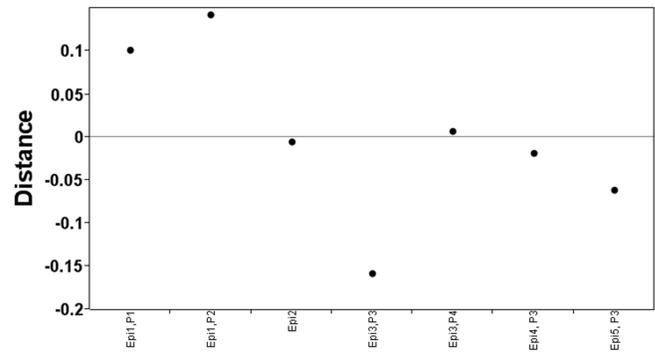


Fig. 8. Comparison of the distance method applied to our layout DOE, gate formation tools, material growth DOE, and gate etch tool.

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ACRONYMS

- FET: Field Effect Transistor
- I_d : Drain current
- I_{dss} : Drain current (I_d) with source and gate voltage of zero
- DOE: Design of Experiment
- V_p : Pinch-off voltage
- V_T : Threshold voltage
- BiFET: Bipolar-field effect process
- HEMT: high electron mobility transistor
- pHEMT: pseudomorphic high electron mobility transistor