Fabrication of III-V Virtual Substrate on 200 mm Silicon for III-V and Si Devices Integration

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Abstract

We present the hetero-epitaxy of III-V materials on 200 mm Silicon wafers by MOCVD. A Ge layer is first grown on the silicon wafer by a two-step process, allowing a lattice matched GaAs layer to be grown on top. Anti-phase boundaries formation are avoided by using a high growth temperature and an arsine partial pressure above 5 mbar during the nucleation of the GaAs layer. The resulting GaAs virtual substrate has a high crystalline quality and a thickness uniformity below 2% over the 200 mm diameter wafer. InGaAs HEMT structure has been subsequently grown using the strain relaxed buffer technique. The measured mobility is 5960 cm^2/Vs with a 2DEG sheet density of 1×10^{12} $/cm^2$. This structure is promising for the hetero-integration of III-V devices with Si CMOS.

INTRODUCTION

III-V substrates such as GaAs or InP are limited in size due to the difficulty in obtaining a low defect density over a large area. Furthermore, the cost of large III-V wafers is much higher than a silicon wafer of the same size. A III-V virtual substrate on silicon can be used to integrate both III-V devices and silicon devices. This integration would enable new integrated circuits both for the “More Moore” approach by combining high-mobility n channel MOS transistors with p-channel Si(Ge) MOS, and for the “More than Moore” approach by combining III-V circuits such as RF, optical and/or high power circuits together with a Si CMOS logic part.

The growth of III-V on silicon substrate is challenging because of lattice and thermal expansion mismatches between the III-V layer and the silicon substrate, and because of the III-V and group IV interface which favors the formation of anti-phase boundaries (APB).

Due to its industrial acceptance and faster growth rate, MOCVD is favored over MBE. However, the GaAs on Ge growth technique that is used by MBE[1] (low temperature migration enhanced epitaxy) cannot be applied in an MOCVD reactor. The growth of GaAs on Ge by MOCVD is still a topic under study and an abrupt interface without growth defects is still not mastered[2], [3].

Here, we demonstrate the growth of GaAs on a 200 mm Silicon wafer using a Ge buffer layer. Both layers are grown in an industrial AIXTRON Crius MOCVD reactor. The resulting 1 µm thick GaAs layer has a thickness uniformity of 1.9%. Its crystallographic quality is assessed by high resolution XRD and room temperature PL measurement. Next, we use this GaAs on Silicon template to fabricate an InGaAs HEMT structure by employing an InAlAs composition graded buffer.

EXPERIMENTAL PROCEDURE

200 mm <100> orientated Si wafer with a 6° offcut towards the nearest (111) plane from AXT were chemically cleaned by SC1 and SC2 solutions followed by an HF dip. The Si wafers were baked at 1050°C under 400 mbar of H_2 for 10 minutes to desorb any contaminant before growth. The Ge buffer layer was grown using a two-step sequence of 100 nm of Ge grown at 400°C and 900 nm Ge grown at 650°C. An annealing at 850°C and 680°C for 10 minutes each was then performed in the reactor chamber in order to decrease the dislocation density.

For III-V growth, the Ge-on-Si wafers were cleaned in DI water with megasonic prior to their reintroduction in the growth chamber. A 5 minutes bake at 630°C under H_2 was performed to remove the Ge native oxide. Then a two-step GaAs layer was grown at 630°C. First, a 100 nm-thick nucleation layer was initiated with varying arsine partial pressure from 0.3 to 5 mbar. Then the GaAs layer was grown at our regular epilayer growth conditions, namely V/III = 46, arsine partial pressure = 0.3 mbar and TMGa flow of 96 µmol/min.

The InAlAs graded buffer was grown at a fixed group III flow of 44.8 µmol/min by varying both the TMIn and TMAl flows linearly. The V/III ratio during the graded buffer growth was kept constant at 50. The composition of the graded buffer varies linearly from AlAs to InAlAs with a grading rate of 1.4% misfit/µm.

The HEMT stack was grown at 630°C and was targeted to be lattice matched to the graded buffer capping layer. The n-type doped InGaAs contact was grown using Si_2H_6 as doping gas with Si_2H_6/group III ratio of 6.5×10^{-3}, leading to an electron concentration of 4×10^{18} cm^{-3}, as measured by Hall effect.

EXPERIMENTAL RESULTS AND DISCUSSION

1) GaAs-on-Silicon

We first optimized the growth of GaAs on pure Ge wafers. The arsine partial pressure has a strong influence on the GaAs surface morphology, as shown in Table 1. A high V/III ratio is not a sufficient condition to obtain a smooth and APB-free GaAs layer. Indeed, we have found that a minimum arsine partial pressure of 5 mbar is necessary to obtain smooth GaAs free of APB.

TABLE I
THE INFLUENCE OF THE ARSINE PARTIAL PRESSURE DURING THE GAAS NUCLEATION LAYER GROWN ON GE SUBSTRATE

Arsine partial pressure (mbar)	**V/III ratio**	**Surface appearance**	**Presence of surface pits under optical microscope**
0.3	234	Hazy	Yes
1.25	936	Hazy	Yes
2.5	936	Specular	Yes
5	936	Specular	No
5	468	Specular	No

We have then successfully transferred this growth recipe to the Ge-on-Si substrate in order to obtain a 200 mm virtual GaAs wafer. As shown in Figure 1.a, the cross section TEM image shows that the GaAs layer is free of APB and no dislocation are observed in this sample. The dislocations are confined at the Ge/Si interface and do not propagate into the GaAs layer.

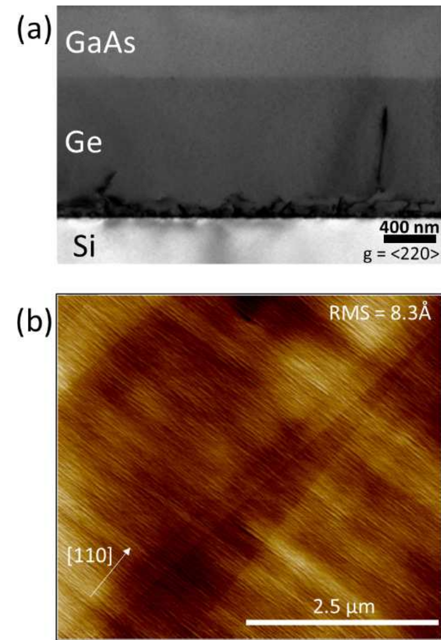

Figure 1: (a) : (a) Cross-sectional transmission electron microscope image of the GaAs on Ge-on-Si sample. The interface between GaAs and Ge is abrupt and free of crystalline defects. We do not detect any anti-phase boundaries in the GaAs layer. Misfit dislocations are visible at the Ge/Si interface with one threading dislocation segment extending in the Ge layer. (b) 5x5 μm^2 AFM image of the surface of the GaAs/Ge/Si sample. The root mean square roughness is 8.3Å.

Owing to the small lattice mismatch between GaAs and Ge (<0.1% at room temperature), we expect the threading dislocation density in the GaAs layer to be similar to the one in the Ge layer underneath. We have previously measured the dislocation density of the Ge layers [4] to be less than 5×10^7 cm^{-2}. This density of defects allows for the fabrication of majority carrier devices (HEMT for instance) that are less sensitive to dislocation density than minority carrier devices. The AFM scan in Figure 1.b shows the smooth surface of the GaAs layer. The measured root mean square (RMS) roughness of a 5µm × 5µm scan is 0.83 nm.

The thickness uniformity of the GaAs layer as measured by spectroscopic ellipsometry is depicted in Figure 2. For this particular sample, the average GaAs layer thickness is 1041 nm with a standard deviation of 20 nm on a series of 49 measurement points.

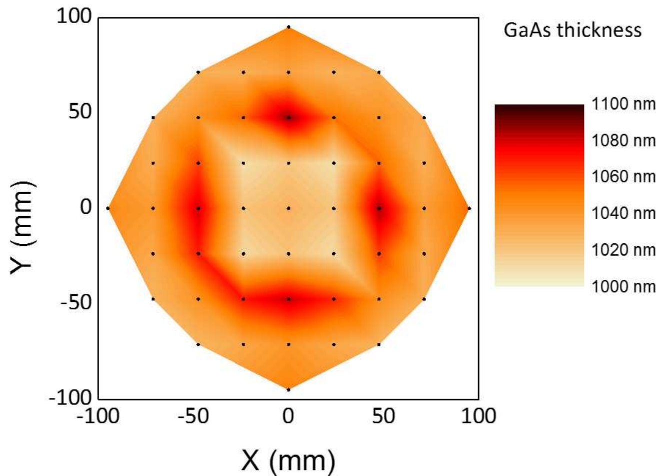

Figure 2: GaAs layer thickness mapping on the 200 mm wafer measured with spectroscopic ellipsometry. The average GaAs layer thickness is 1041 nm and the standard deviation is 20 nm.

The crystalline quality of the GaAs layer has been assessed by high resolution XRD. The FWHM of the GaAs (004) peak measured in a rocking curve configuration (ω-scan) is 196 arcsec. This value is comparable to the lowest values reported in the literature [1], [5].

Room temperature PL measurement shown in figure 3 confirms the high optical quality of the GaAs layer. The full width half maximum (FWHM) of the GaAs peak emission is 31 nm (or 49 meV) which corresponds to the band-to-band recombination.

2) InAlAs graded buffer

InAlAs buffer with a linearly graded composition from pure AlAs to $In_{0.30}Al_{0.70}As$ or $In_{0.52}Al_{0.48}As$ were grown on top of the GaAs virtual substrate. For the later, a composition overshoot was used: the composition was graded up to $In_{0.60}Al_{0.40}As$ and then capped by an $In_{0.52}Al_{0.48}As$ layer followed by a thin InP layer. In Figure 3, the XRD reciprocal space map around the (004) plane of one sample is shown. We can see the diffraction peaks from the silicon substrate, the Ge and the GaAs layer. The InAlAs graded buffer produces a continuous diffraction peak extending from the GaAs peak to the InP peak. Using the analysis of the (004) and the (224) RSMs, we have calculated the composition of the cap layer to be 51.7% and its in-plane strain to be -0.04%, meaning that the in-plane lattice constant is smaller than the relaxed value at that composition (tensile strain).

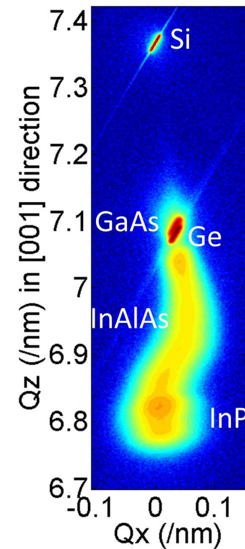

Figure 3: XRD reciprocal space map taken around the (004) reflections. The sample consists of a 3µm thick InAlAs graded buffer grown at 630°C capped with a 10 nm InP layer.

The surface morphology of this sample was analyzed by AFM. As displayed in Figure 4, the surface is very rough with a cross-hatch pattern originating from the misfit dislocation array in the graded buffer[6]. The peak to valley depth is around 300 nm.

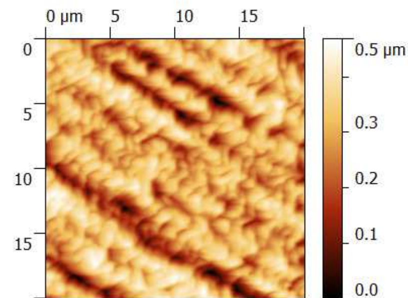

Figure 4: 20x20 µm^2 AFM scan of the Si/Ge/GaAs/AlAs/InAlAs/InP sample. The surface appears rough with long range oscillation with an apparent wavelength of 2.3 µm, originating from the misfit dislocation arrays. The peak to valley depth of these surface oscillations is around 300 nm. The RMS roughness of 76 nm.

In order to understand the origin of the rough surface, this sample was observed by TEM in cross section (Figure 5). The dislocations are visible in the graded buffer up to 2.6 µm from the GaAs layer, which corresponds to a composition of approximately $In_{0.45}Al_{0.55}As$. After this point, a dark contrast is observed which is attributed to the onset of phase separation in the growing material [7]. The phase sepatation contributes to the increasing roughness of the growing layer. The quality of the capping layer is not suitable for device fabrication due to the high roughness.

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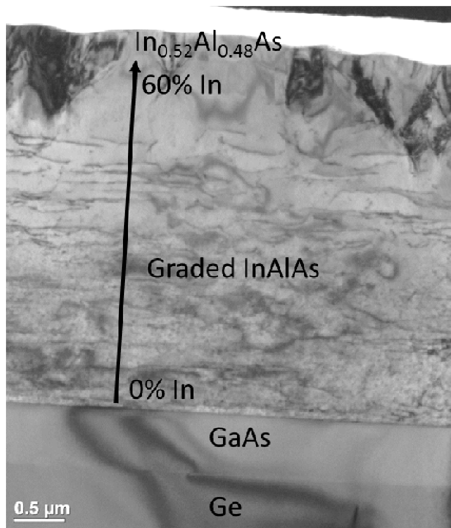

Figure 5: TEM image of the InAlAs graded buffer on silicon substrate. The misfit dislocation are visible in the InAlAs graded buffer. The high contrast at the top of the graded buffer is ascribed to the phase separation occuring in the InAlAs with In composition of around 40%, thus creating a rough surface.

In order to avoid the phase separation and to obtain a smoother layer, a sample has been grown with an InAlAs composition that was graded up to $In_{0.30}Al_{0.70}As$. The growth temperature (630°C) and strain gradient (1.4%misft/µm) were kept the same. For this sample, no composition overshoot was used.

The AFM scan of this sample is shown in Figure 6. The surface morphology is smoother than the previous sample, because the phase separation was prevented. The RMS roughness is 10.6 nm with peak to valley depth of 81 nm.

The micrometer scale wavelength oscillations are due to the misfit dislocation array in the graded buffer. This long range roughness is not detrimental to the fabrication of devices in which the active region is less than the roughness wavelength.

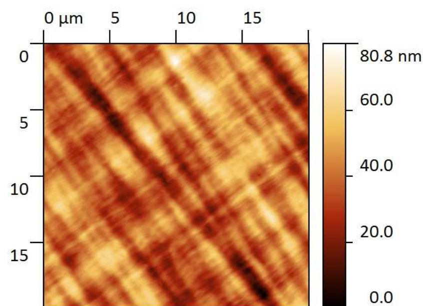

Figure 6: Surface morphology of a graded buffer sample with a final InAlAs compositon of 30%. The cross-hatch pattern is visible along the <110> directions. The peak to valley depth is around 80 nm and the RMS roughness of this scan is 10.6 nm.

The XRD analysis of the 30% InAlAs sample has been performed and the cap layer composition was measured to be 28.9% with a strain value of -0.25% (in the [110] in-plane direction).

3) *InGaAs HEMT*

A lattice-matched InGaAs HEMT structure was grown on top of the 30% In graded buffer. The structure comprises an InGaAs channel of 10 nm thickness and an InAlAs barrier. A Si delta doping layer is grown 7 nm below the channel. The contact layer is a highly doped n-type InGaAs (Figure 7).

$In_{0.30}Ga_{0.70}As$ cap - 60 nm
$In_{0.30}Al_{0.70}As$ barrier - 25 nm
$In_{0.30}Ga_{0.70}As$ channel - 15 nm
$In_{0.30}Al_{0.70}As$ spacer - 7 nm
$In_{0.30}Al_{0.70}As$ - 500 nm
InAlAs graded buffer
GaAs
Ge
Si substrate

Figure 7: Schematics of the InGaAs HEMT structure grown on silicon substrate

The cross section TEM of the structure is shown in Figure 8. Contrary to the previous case, in which the InAlAs buffer composition was graded up to 60% In, the current composition grades up to 30% In. There is no trace of phase separation in the sample, and no threading dislocations were observed in the device layers, setting up an upper bound of the threading dislocation density to 10^8 cm^{-2}.

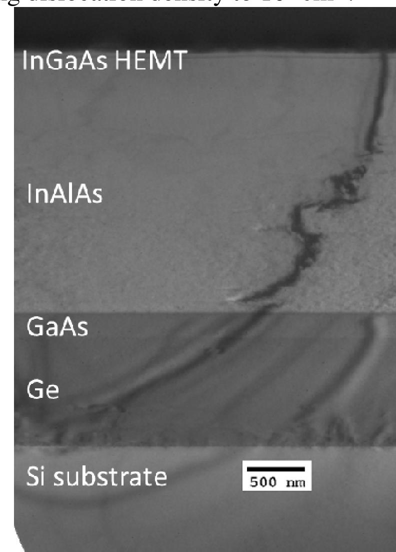

Figure 8: Cross-sectionnal TEM image of the InGaAs HEMT structure on Silicon. The final InAlAs graded buffer concentration is 30% In. The InGaAs HEMT structure consists of a 15 nm InGaAs channel

Hall Effect measurement samples have been prepared using Indium contacts and a citric acid:hydrogen peroxide 1:1 solution was used to etch selectively the InGaAs cap with respect to the InAlAs barrier. A maximum mobility of 5960 cm^2/Vs has been measured, together with a 2DEG carrier density of 1.0×10^{12} cm^{-2}.

CONCLUSIONS

III-V materials have been integrated with a 200 mm silicon substrate using an industrial MOCVD reactor. We have demonstrated the fabrication of a GaAs virtual substrate with a low roughness, a high crystalline quality and the absence of anti-phase boundaries. Next, an $In_{0.30}Ga_{0.70}As$ HEMT has been grown using an InAlAs composition graded buffer. The threading dislocation density is below 10^8 cm^{-2} and the Hall mobility of the structure is 5960 cm^2/Vs with a carrier density of 1.0×10^{12} cm^{-2}. This structure holds great promise for the fabrication of III-V devices on silicon substrate.

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ACRONYMS

AFM: Atomic Force Microscopy
HEMT: High electron mobility transistor
MBE: Molecular Beam Epitaxy
MOCVD: Metal organic chemical vapor deposition
MOVPE: Metal organic vapor phase epitaxy
PL: Photoluminescence
TEM: Transmission Electron Microscopy
XRD: X-Ray Diffraction