SiC / GaN via process – in search for perfection

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Abstract

SiC/GaN via etch and via loop process integration were studied. A new etch process region has been developed that produces nearly perfectly smooth via side wall. Side effect of other processes in the via etch process flow was minimized for improved via quality.

INTRODUCTION

Interest in GaN devices in the semiconductor industry for high power applications has increased in recent years. For example, nearly fifty percent of the papers presented at the CS MANTECH conference in 2014 were GaN related. GaN has high breakdown voltage, high electron mobility and saturation velocity [1], making it a very attractive material for many applications including high-power, high speed, and high-temperature microwave applications [2-3].

Although excellent in electric performance, GaN device has its own challenges in some of its device fabrication processes. For example, the majority of GaN devices were developed using SiC as the substrate for GaN epitaxial growth. The etch rate of SiC is still limited to approximately 1 um/min, much lower than that of GaAs (GaAs etch rate can easily be made to ~ 6 um/min or higher). The slow etch rate of SiC means that a robust etch mask is needed for the backside SiC and GaN via etch process. Depending on the etch process conditions, up to ~8-10 um metal hard mask is used for the via etch [4,5]. SiC/GaN via formation utilizing a metallic hard mask makes the overall via formation process much more difficult than that for GaAs vias.

For example after the etch, a layer of etch by-products containing metal can form inside the via along the via side wall due to the use of certain metal etch masks. One may use a wet etch chemical to remove the metal containing by-product after SiC etch and before the GaN etch. However, doing so would very likely also etch away the metal mask. As previously reported [6], removing the metal mask before the GaN etch can potentially introduce an undesired notching effect at the bottom of the via. In addition, it is not uncommon to observe a rough via side wall. A rough via side wall can potentially trap residue inside the via and cause potential issues in the subsequent conformal via side wall metallization.

It would therefore be preferable that the by-product formation on the via side wall is minimized; and secondly, the by-product, once formed, be removed without using a wet etch process that can also attack the hard mask or the metal pad under the via. To be able to remove the by-product without a wet etch process, it is desirable that via side wall be made smooth, especially if the lateral dimension of the via is much smaller than its depth. Typically, a larger via diameter can have a higher etch rate, making it easier to produce. A smooth via side wall will facilitate more effective removal of the by-product without utilizing a wet etch process.

In this paper, we report the results of an improved SiC/GaN via formation process with a very smooth via side wall for small diameter vias in 100 um thick SiC substrates.

EXPERIMENT

Most of the process studies reported in this paper were conducted on 100 mm GaN wafers with the GaN grown on SiC substrates. After completing the front-side device fabrication processes, the SiC substrate was then ground and polished to its final thickness (typically 50 um to 100 um). A via pattern of various diameter sizes were formed on the SiC surface. A via metal etch mask was deposited onto the SiC surface. The optimized process was extensively evaluated on multiple production wafers to demonstrate process repeatability.

For the SiC/GaN via etch, an inductively coupled plasma (ICP) etch tool with an optimized ICP source was used. Details of the SiC etch processes have been previously reported [7-8]. A variety of new etching conditions were evaluated in this study using a number of parameters including reactant composition (different gas species and different gas flow rate), process pressure, RF power, and wafer-to-plasma source spacing.

An optical microscope was used for general via inspection. For a more detailed analysis, the via was analyzed using SEM, FIB, and EDX to characterize the via shape, via side wall surface topography, and the chemical composition at the via side wall surface.

RESULT

It is worth to note that the sample preparation appears to have a substantial effect on the quality of the etched via. This is shown in Figure 1, where the via for both Figure 1(a) and Figure 1(b) were etched under very similar etch conditions.

The via side wall is substantially different between the two samples. This is believed to be primarily due to a variation of the via etch mask. The via hard mask shown in Figure 1(a) has a better defined circular shape, while the top surface of the via perimeter shown in Figure 1(b) is rougher than that of Figure 1(a). Bearing this potential variation of the etch mask in mind, subsequent etching process optimization was done using samples cut from the same wafer.

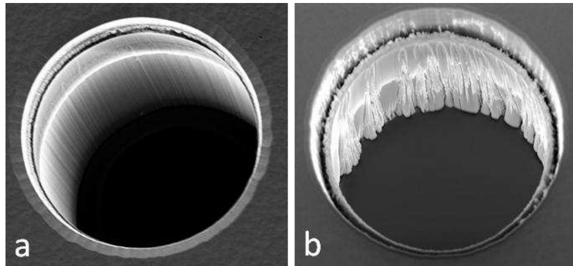

Figure.1. Via from two different wafers etched under similar conditions.

Figure 2 compares vias etched under two different etch conditions for samples cut from the same wafer (these samples were not cleaned after etch). As shown in Figure 2(a), the via side wall was very rough under an un-optimized etch condition. While Figure 2(b) shows the via side wall became much smoother as the etch condition was moved to a more optimized process. This demonstrates the effect of the etching condition on the quality of via side wall. The improvement in the etched vias observed on the small samples (Figure 2(b)) was repeated on whole wafers as shown in Figure 3.

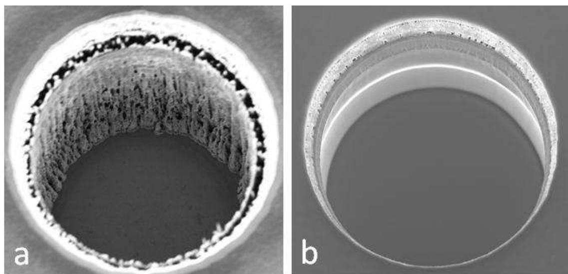

Figure 2. Via from two samples cut from the same wafer but etched under two different conditions. (a) sample etched under an un-optimized condition; (b) sample etched under an optimized condition.

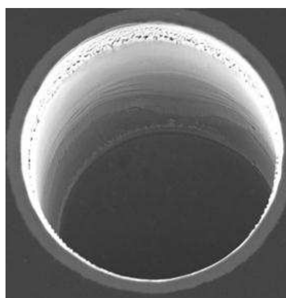

Figure 3. Typical via on whole wafers etched under an optimized condition.

Several vias were cross-sectioned to examine the via formed by the optimized process. Examples of the cross-section views are shown in Figure 4 and Figure 5. In Figure 4, some of the filling material inside the via is an artifact of lapping process before imaging. In Figure 5, the top is a section of the via making contact with the front side metal as circled in Figure 4; the bottom is a magnified view near the corners of the via.

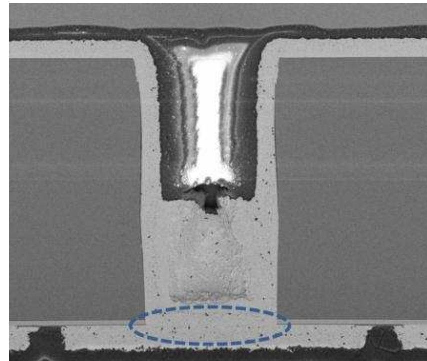

Figure 4. Cross-section of a completed via.

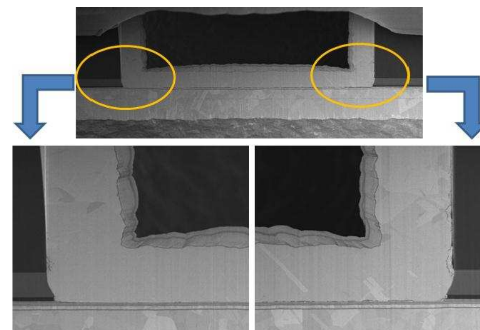

Figure 5. FIB-cross section of the bottom of the via.

Figure 2(a) and Figures 3-5 show that the side wall of the via etched using the optimized process is smooth, and the overall via profile and contact with front side metal is excellent. Additional analysis using EDX indicates that there is no appreciable amount of foreign materials or by-products left on the via side wall after a gentle clean. This can be seen in Figure 6, where the EDX signal only showed the presence of Si and C, the primary composition of SiC.

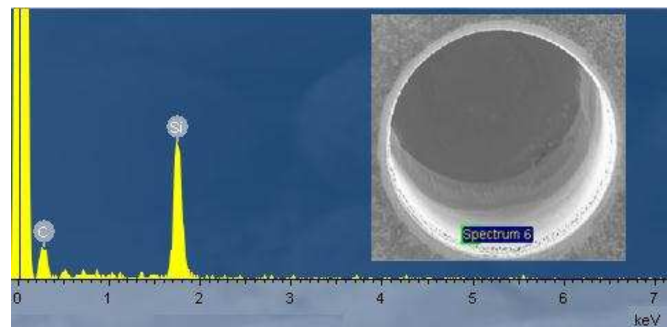

Figure 6. EDX spectrum of via side wall.

DISCUSSION

The results presented previously shows that although in most cases SiC / GaN via can be free of pillar defects [6], the via side wall can be rough under un-optimized etching conditions. As the etching process is moved to a more favorable etch condition, the via side wall can be substantially smoothened in addition to being free of pillar formations at the bottom of via. The via side wall can also be free of foreign materials and by-products as confirmed by EDX spectrum analysis. However, in practice, it is not convenient to monitor the etch result using SEM for all wafers and for all vias in a production environment. We note that in most cases, an optical inspection can easily reveal the quality of via side wall without much ambiguity. A via with rough side walls often does not have a well-defined shape as the original via pattern, while a via with smooth side walls maintains the shape of its original pattern as shown in Figure 7. The circular pattern was significantly distorted as shown in Figure 7(a) due to the side wall roughness. For vias with smooth side walls, the via at the bottom maintains a perfectly circular shape as shown in Figure 7(b).

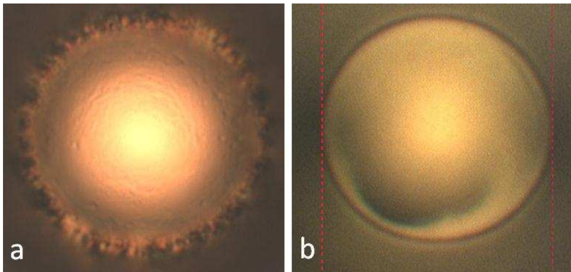

Figure 7. Optical images of via focused at the bottom after the SiC / GaN etch. (a) Via with rough side wall, and (b) via with smooth side wall.

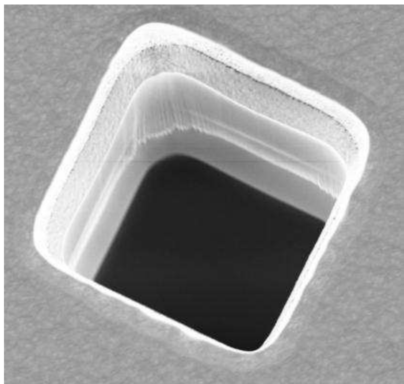

Figure 8. SEM image of a square via with aspect ratio of 3.

Figures 2-7 are for via with aspect ratio ~ 2, where the aspect ratio is the ratio between via depth and via diameter for a circular via, or between the via depth and the via width for square or rectangular vias. The optimized etch process can extends well to higher aspect ratio vias, Figure 8 is an example of square via with aspect ratio of ~3. The via side wall is smooth and the bottom of the via is substantially free of pillar formation.

CONCLUSION

Various factors such as the via hard mask can have a significant effect on the via side smoothness. A new etch process has been developed that produces nearly perfect smooth via side walls and is less sensitive to other variations such as the via etch mask. This etch process has been demonstrated to be applicable to small vias in the SiC substrate with an aspect ratio of 3. It is also shown that a very simple optical inspection can be used as a first gauge of the via side wall quality without utilizing SEM inspection. This substantially simplifies the in-line inspection process in a production environment.

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ACRONYMS

ICP: Inductively Coupled Plasma
EDX: Energy-dispersive X-ray spectroscopy
SEM: Scanning electron microscope
FIB: Focused ion beam