Analysis and Optimization of a Through Substrate Via Etch Process for Silicon Carbide Substrates

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Abstract

Through substrates vias (TSVs) are an important design feature to facilitate chip mounting and to enhance electrical performance especially at high frequencies. To process TSVs in silicon carbide (SiC) as base material, the SiC wafers are bonded by means of a temporary wafer bond process to a supporting carrier, thinned to the desired target thickness, furnished with an etch mask, and then etched by means of a plasma etch process.

We have analyzed the stress in the wafer stack due to the bonding and plasma etch processes. We found that the stress in the wafer-carrier sandwich due to bonding originates mainly from the different coefficients of thermal expansion of the materials. The bow of the wafer-carrier composite during the etch process in the plasma reactor was measured in real time with an on-line sensor. The effects of the mechanical fixation of the composite in the reactor and of the helium back pressure as well as the impact of the etch plasma could be determined independently. This allowed to develop an etch process that exerts less stress and minimizes mechanical failure of the wafers.

INTRODUCTION

Through substrates vias (TSVs) are an essential feature to realize high frequency micro strip circuits. Moreover, they facilitate chip mounting significantly. While for gallium arsenide (GaAs) MMICs via processes are in routine use, the corresponding process versions for GaN-based transistors and MMICs are less common. As GaN is often epitaxially grown on SiC wafers, the processing of TSVs involves the preparation of holes in SiC and GaN. Compared to silicon and GaAs, these materials are much more difficult to etch and require rather harsh etch conditions. FBH has developed and implemented a process flow for the fabrication of TSVs in SiC wafers for GaN-based power transistors and MMICs. The TSV back side process is performed after completion of the front side process. The 100 mm wafers are bonded to a 105 mm supporting wafer with HT10.10 as temporary adhesive. The SiC wafers are then thinned by lapping and polishing to their desired thickness of 100 µm. The etch mask for the via etch process consists of a 500 nm thick aluminum (Al) and a 3000 nm thick indium tin oxide (ITO) layer. This material combination allows the plasma etching of vias in 100 µm thick SiC with sizes down to 20x80 µm². The etch process is performed in a Sentech SI500 ICP etch chamber with a sulfur hexafluoride/helium gas mixture. Then, the remaining mask is stripped in diluted potassium hydroxide and the GaN-based epitaxial layer is etched in another SI500 ICP tool using chlorine plasma. After deposition of a titanium/gold plating base, 5 µm of gold are electroplated. Finally, the wafer is debonded from the carrier, cleaned and diced. The cross section of a typical via obtained with this process is shown in fig 1. Typical values for the electrical resistance of a single via are about 10-20 milliohm.

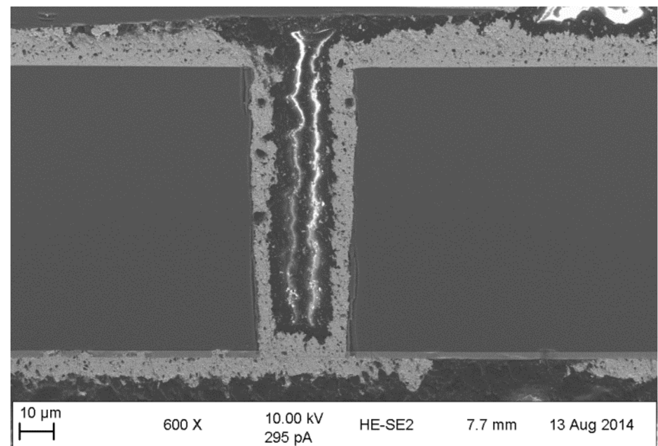

Fig. 1 Cross section of a TSV in 100 mm SiC obtained with FBH's via process. The TSV is electrically connecting the back side (top) to the source contact on the front side of the wafer (bottom).

CHALLENGES

SiC is mechanically very hard and chemically rather inert, which makes plasma etching of TSVs very difficult [4,5,6] even if the wafer is thinned to 100 µm. Etching mask, carrier material, ICP and RF power density, and process temperature strongly affect the result. To sustain a productive etch rate, platen temperature and reaction heat

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have to be as high as possible without causing delamination of the thinned wafer from its carrier. Due to the low etch rate in the order of 0.5 µm/min, a long term resistant hard mask is required. The material of the support wafer must be transparent to allow for lithographic access of the wafer's front, must provide efficient and uniform heat conduction, and it must have a similar coefficient of thermal expansion to avoid excessive stress when etching SiC at elevated temperatures. The fixture of the composite consisting of the wafer and the support wafer has to allow for temperature control by cooling using helium flow at the back, uniform etching, and minimum mechanical stress on the wafer.
To study the impact of the various parameters on the wafer bow and hence the stress in the system, an independent measurement of their impact on the wafer bow in the etch chamber is required.

RESULTS AND DISCUSSION

Analysis of the bonding process

To allow thinning and processing of the thinned wafer, bonding to a carrier wafer for mechanical support is required. In this bonding step any damage of the structures on the front side, especially of the delicate air bridges that may be present, has to be avoided. A potential mechanical damage of these air bridges (change in height) is difficult to detect; any residues that may be present under the bridge are in principle not detectable by optical inspection. Furthermore, there is a certain spread of the exact form of the bridge across the wafer. We developed a test structure that allows for quick electrical determination of the result of the overall process. The break through voltage of test air bridges of different span is measured before and after process. Any significant deviation indicates either residues below the bridges or mechanical stress and shape change.
The air bridges need protection during the bonding process. As bonding material the spin on material HT10.10 (Brewer Science) with a nominal thickness of 22 µm was used. However, this thickness was not sufficient to protect air bridges of 6 µm height reliably. A two step coating process with an intermediate soft curing proved to be sufficient to avoid any changes in the break down voltage of the test structures. This double coating also alleviated the debonding step after the process.
Wafers were bonded in an EVG501 bonder with a bonding pressure of 3N/cm² at 180 °C for 2 min and removed from the tool after cooling to 100 °C. During the bonding process a background chamber vacuum better 5µbar was kept. The support wafers have a diameter of 105 mm and a thickness of 1 mm; the 4 inch process wafer is bonded in the center. Two carrier materials have been tested: Glass carriers with a coefficient of thermal expansion (CTE) of 3.3 ppm and sapphire carriers with a CTE of 8.5 ppm. SiC has a CTE of 4.5 ppm. This gives a concave bow for the glass – SiC composite and a convex bow for the Sapphire – SiC composite at room temperature after the bonding process. The respective center bow was about 42 µm and 122 µm. Fig. 2 shows a typical example for the measured bow of a 525 µm thick SiC wafer bonded on a 1000 µm thick glass carrier with HT10.10 at 180 °C process temperature as determined by white light interferometry.

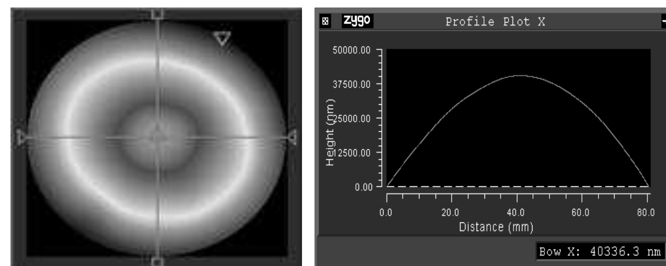

Fig. 2 Bow of a 525 µm SiC wafer bonded on 1000 µm glass carrier with HT10.10 at 180 °C process temperature as determined with white light interferometry at room temperature.

Bow and stress in a multilayer system depend on the bonding temperature, the thickness of the respective layers, their Young's moduli and their coefficient of thermal expansion and can be calculated as described in [1].

Table 1 Parameter set for the calculation of bow and stress

Material	CTE/ppm K^{-1}	Thickness/µm	E/GPa
SiC	4.5	525	450
HT10.10	45	35	5
Glass	3.3	1000	70

The thickness of the bonding material HT10.10 is much lower than the thickness of the wafer and the carrier. It is also the least stiff material and its contribution to the bow of the system can hence be neglected in a very good approximation.

However, simulated and measured bow values do not match if the process temperature of 180 °C is taken into account. The measured bow is always much lower than the calculated value. From our experimental data we can derive the bond temperature, i.e. the temperature at which the materials adhere sufficiently to avoid further gliding. With the parameter set given in Table 1, a bond temperature for SiC on glass of about 80°C was calculated. However, a bonding process carried out at 80 °C did not yield sufficient bond quality.

Etch mask evaluation

A nickel, an Al and an Al/ITO etch mask were tested for etching of vias holes into the SiC wafer. The nickel mask was obtained by deposition of a plating base, formation of 3 µm high columns in PGMI and electroplating of 3 µm of nickel from a nickel sulphamate bath, followed by a lift-off step. The Al mask was created by the same process scheme, but Al was deposited by evaporation. However, these two mask materials showed disadvantages in FBH's process line. The nickel mask created a lot of particles in the etch

chamber and the Al mask showed strong pitting with our etch process.

We developed a layered etch mask stack that consists of a 500 nm Al layer followed by 3000 nm ITO layer. The Al layer facilitates the lift-off process in potassium hydroxide after completion of the etch process, as the Al dissolves within about 10 min in the alkaline solution. It also prevents any UV radiation from the etching process to reach the bonding layer. The typical mask loss as monitored by in-situ interferometry is plotted in fig. 3. An ITO thickness of 3000 nm is sufficient for a process time of 3 hours.

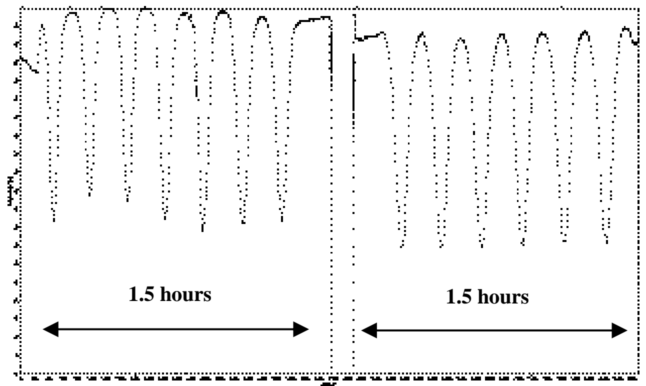

Fig. 3 ITO mask loss rate during the SiC etch process as monitored by in-situ interferometry during the etch process. The gap after 1.5 hours is caused by an interruption of the process for intermediate inspection.

Analysis of the etch process

Fig. 4 depicts a cross section of the wafer holder in the etch tool. The support wafer is clamped along its perimeter, no mechanical stress is exerted on the thinned process wafer in the center of the carrier wafer. Channels in the bottom part of the carrier allow gas flow for heat regulation.

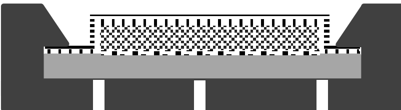

Fig.4 Wafer holder. The holder is made from Al and clamps the support wafer at the perimeter. The etch mask is electrically connected to the holder. Channels in the back allow for cooling gas flow.

To access the mechanical distortion of the system wafer-carrier in the plasma etch chamber during etching, a commercially available wafer bow metrology system (EpiCurve®, LayTec AG) was used. This system was originally developed for controlling the epitaxial growth in high temperature MOCVD reactors. For this study it was adapted to fit to FBH's Sentech SI500 ICP etch chamber that provides a glass window in the center of the top. The curvature measurement system (fig. 5) consists of a light source unit that directs two parallel laser beams towards the wafer surface. If the wafer is bent, the distance between the reflected beams changes; this distance is evaluated by the system and allows to calculate the center bow.

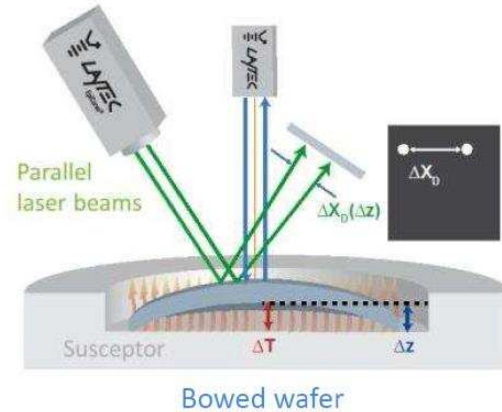

Fig. 5 Sketch of the wafer curvature measurement system.

As an example fig. 6 shows the impact of the pressure of the helium at the back side on the bow of a 525 µm thick 100 mm SiC wafer bonded to a 105 mm diameter 1000 µm thick glass carrier. The bow linearly increases with increasing pressure up to 60 µm.

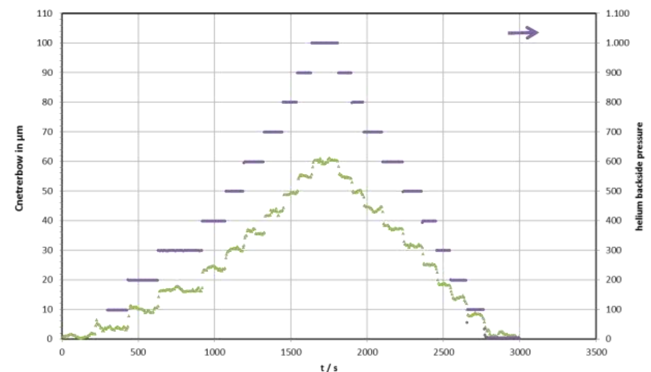

Fig.6 Impact of helium back pressure on bow of a 525 µm thick 100 mm SiC wafer bonded to a 1000 µm thick glass carrier.

Surprisingly, the measured values match exactly the calculated values for a thin circular plate that is not clamped at the edges but only supported. This means that from a mechanical point of view the wafer holder in the etch tool does not rigidly fix the supporting wafer.

Fig. 7 shows the course of the bow after optimization of the etch process parameters. The back side pressure of the cooling gas was reduced to 300 Pa. The platen temperature was kept at 100 °C. Initially, the carrier is heated with maximum power (blue scale), but during the etch process the necessary power is reduced due to the exothermic etch

reaction. During heating the wafer-carrier composite still undergoes significant shape changes as indicated by the center bow (green dotted line). At the beginning the system bows and relaxes until the plasma is switched on. Then the bow increases again. However, the bow is now less than 40 µm during the whole process and no impact on the wafer-carrier composite is observed after the process.

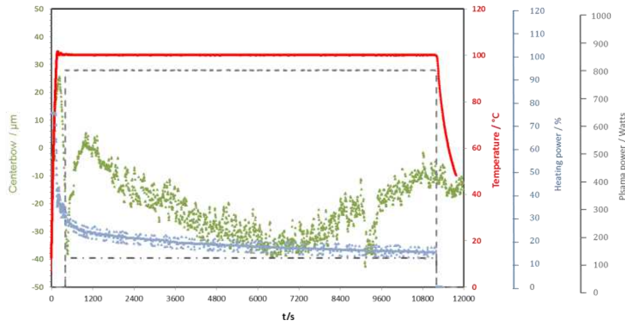

Fig.7 Wafer bow during the optimized SiC etch process of a 100 µm thick SiC wafer bonded to a 1000 µm thick glass carrier.

We found a sweet spot for the etching with a sulfur hexafluoride/helium mixture applying an RF ICP power of 750 and a RF platen power of 150 W, a platen temperature of 100 °C, a chamber pressure of 2.5 Pa, and a helium back side pressure of 300 Pa. The etch rate at the beginning of the process is 48 µm/hour decreasing to 30 µm/hour at a via depth of 100 µm.

CONCLUSIONS

The application of the in-situ measurement system allowed bow measurement of the wafer-carrier composite in the plasma etch chamber during etching. An independent determination of the contributions of the helium back flow, heating of the platen, ICP and RF plasma power, and mechanical clamping on the wafer bow in the etch chamber was possible. This knowledge allowed to optimize the etch process by minimizing the stress on the thinned wafer, hence decreasing risk of cracks and increasing the yield of the process.

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ACRONYMS

CTE	:	coefficient of thermal expansion
MMIC	:	monolithic microwave integrated circuits
ICP	:	inductively coupled plasma
TSV	:	through substrate vias
ITO	:	Indium tin oxide
E	:	Young’s modulus
PMGI	:	Polymethylglutarimide