Simulation of the Impact of Through-Substrate Vias on the Thermal Resistance of Compound Semiconductor Devices

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Abstract

The impact of through-substrate vias on the thermal performance of compound semiconductor devices requires careful consideration in the design of high-power RF devices. In this paper, the results of a comparative study employing thermal simulation that contrasts a variety of via types and configurations is presented. Specifically the study compares via types including; end-, slot- and segmented slot-vias against a baseline case of no through-substrate vias. The study also covers a range of via fill types and substrate materials in common use today including; GaAs, Si and SiC.

INTRODUCTION

MACOM is fortunate to have one of the broadest power transistor technology portfolios in the industry today, including devices based on the Si, GaAs, GaN-on-Si and GaN-on-SiC materials systems. While each of these technologies offer unique benefits within the performance-cost trade-space, a challenge common to all is the requirement that operational temperatures be maintained at levels that can assure long-term reliability of their associated components. Consequently, significant engineering time and attention are often applied to thermal design matters. On the performance side, the use of through-substrate vias to achieve minimal die size and increased gain by way of lowering ground inductance has been commonly applied throughout the industry for several decades, and the sophistication of associated process techniques has steadily evolved during that time to enable vias of increasing aspect ratio as well as improved plating uniformity and conformality [1-3]. But use of these performance enhancing structures has the potential to improve and perhaps more importantly, in some cases degrade the overall thermal performance of a device depending upon the specifics of configuration, construction, as well as the substrate material employed. In some cases designers may entirely ignore the thermal impact of these structures, and this is especially of concern in transitioning to newer, less-familiar technologies, such as GaN-based devices that exhibit significantly higher power densities. Here, experiential methods or rules of thumb may not apply and can potentially lead to poor performance and or reliability due to unanticipated degradation of thermal resistances. In this paper a comparative study of how the materials system, via configuration and via type impact device thermal resistance is presented. More specifically, three different materials systems of significance to modern power transistors are compared and contrasted; GaAs, GaN-on-Si and GaN-on-SiC. For via types we consider three types; end-vias - those that reside outside the immediate active region of the transistor, slot-vias - those that make direct contact with the transistor source contacts, and a subset of this latter category referred to as segmented slot-vias. All these are benchmarked against a baseline, no-via case. Lastly we look at the impact of via fill-type to gain insight into the impact of back metallization on via thermal properties.

APPROACH

Power RF products based on the substrate materials mentioned above can span a range of output power levels from Watts to 100's of Watts. For the purpose of this comparative study we chose a common total periphery commensurate with moderate power levels for each of the technologies investigated. Specifically a common total gate periphery of 15.4mm and associate unit gate width of 367μm or 42 gate fingers was utilized for all simulations presented in this work.

For GaAs and GaN-on-SiC technologies a gate-to-gate pitch of 54μm and substrate thickness of 75μm were chosen and die areas were fixed at 1.0 x 2.6mm^2. For the GaN-on-Si cases we increased the gate-to-gate pitch to 65μm while maintaining the total gate periphery and reduced die thickness to 50μm in keeping with the design strategies commonly employed for this materials system. Associate chip size increased commensurately for these cases to 1.0 x 3.0mm^2. Simulations were performed at dissipated power densities applicable for the various technologies and represented the higher range for safe operation - 1W/mm for GaAs and 3.6W/mm for GaN-on-Si and GaN-on-SiC cases.

In all cases, die were simulated assuming attach to a copper-molybdenum-copper (CMC) flange by way of AuSn eutectic with an associated bond line thickness of 38μm. Fig. 1 illustrates the details of the die-to-package stack representative of those used for these simulations, and

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Table I summarizes the various materials and their associated dimensions.

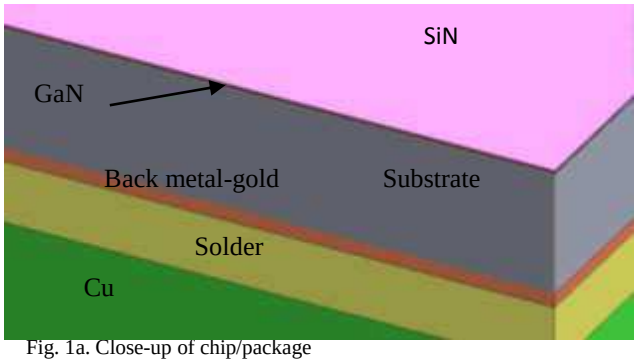


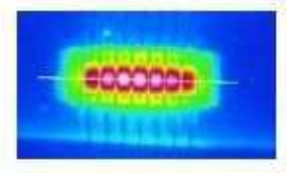
Fig. 1a. Close-up of chip/package

TABLE I
RELATED DIMENSIONS AND MATERIALS

Component	Material	Thickness	Dimensions
Package	CMC	0.5mm/0.5mm/0.5mm	5.8 x 20.3 mm
Solder	Au-Sn	38 µm	chip size
Field Back-metal	Au	8 µm	
Substrate	GaAs,SiC	75 µm	2.6mmx 1 mm
Substrate	Si	50 µm	3mm x 1 mm
Semiconductor	GaN	1 µm	chip size
Front-side passivation	SiN	1 µm	chip size
Via Lining metal	Au	2 µm	

Thermal simulations were performed using ANSYS to conduct three dimensional finite element analysis. Temperature dependent thermal conductivity was taken into account for all of the semiconductor materials within the stack [4], and the impact of epitaxial interfaces were also taken into consideration [5]. Front-side interconnect metallization was deemed inconsequential for the purposes of this comparative study and was not included. For all cases in this study the backside of the CMC flange was attached to an idealized heat sink maintained at 80°C.

Simulations were validated by way of thermal imaging acquired using a Quantum Focus Infrascope II system on devices under DC operation.


Peak Temperature=206.5 C
Fig 2. IR Camera image

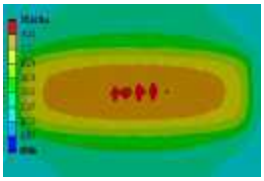

Peak Temperature=205.6 C
Fig 3. Modeled Results

Fig. 2 and Fig. 3 show that the measured vs. modeled peak temperature results compared favorably with IR measurements for the baseline (no-via) GaN-on-SiC case. For this case, the IR imaging registered a peak temperature of 206.5°C, while the simulated equivalent yielded a peak temperature of 205.6°C - thermal resistances of 2.30, and 2.28°C/W respectively. This indicates that the model reflects the experimentally observed values accurately and provides confidence in model predictions.

A total of 36 simulations were performed for the three materials systems. For each of the three materials system, four via types were considered; 1) the baseline case (that representing the no-via case in which down-bonds would be normally used to form connection to ground) depicted in Fig 4a, 2) a 50µm diameter circular end-via case depicted in Fig. 4b, 3) a 30x360µm^2 slot-via (Fig. 4c.), and 4) a segmented variant of the slot-via case whereby two 30x60µm^2 vias contact each source contact pad as depicted in Fig. 4d.

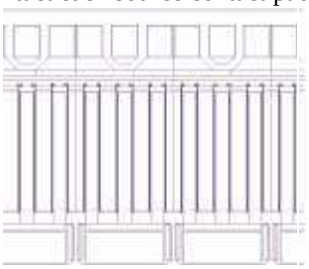


Fig 4a. Baseline no-via case

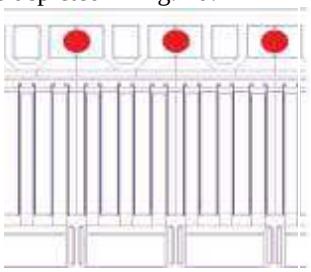


Fig 4b. End-via

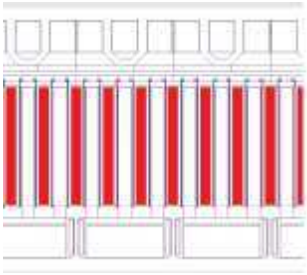


Fig 4c. Slot-via

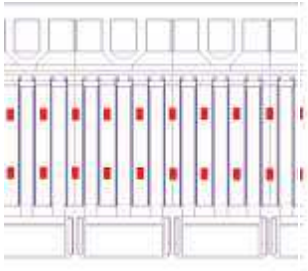


Fig 4d. Segmented slot-via

Additionally, three via fill configurations were modeled: lined-via (Fig 5a.), filled via (Fig.5b.), and via cavity (fig 5c.).

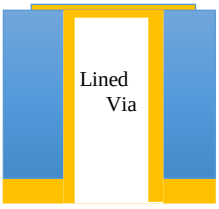


Fig 5a. Lined Via

Fig 5b. Filled via

Fig 5c. Via Cavity

All lined-via cases assumed a perfectly conformal and uniform sidewall metallization comprising 2µm of gold. For the via cavity case, we assumed a zero thickness sidewall metallization. While this latter implementation clearly represents an electrically impractical case, it was employed in this study as a means of establishing worst case

assessment for the lined via cases in that metallization thicknesses can vary from manufacturer to manufacturer.

RESULTS & DISCUSSION

Table-II summarizes the results for cases involving various end via configurations. It is shown that end-vias exhibit negligible thermal impact in comparison with the no-via baseline case for all three materials systems and irrespective of all via fill conditions.

TABLE II.
PEAK TEMPERATURE OF END VIAS TYPES

		END VIAS			
	No via	Au Lined Via	Au-filled	Via- cavity	$\theta_{Thermal\ Resistance}$
GaAs: 1 W/mm	156°C	156°C	156°C	156°C	4.94 °C/W
GaN-on-Si: 3.6W/mm	208°C	208°C	208°C	208°C	2.33 °C/W
GaN-on-SiC: 3.6W/mm	206°C	206°C	206°C	206°C	2.29 °C/W

This makes sense as the end-vias in this study are placed well outside the active region of the die where there is no significant temperature gradient, hence the effect of end-vias are negligible to the overall thermal resistance of these systems.

Just as end-vias are used to improve ground inductance by avoiding the use of bond wires to facilitate that connection, slot-vias are used to further improve ground inductance by connecting the vias directly to the source contacts of a transistor cell and hence lower further the lead inductance component of this parasitic. Table-III summarizes the simulated peak temperature for the various slot-via cases of this study. The no-via baseline case is also repeated here and in following tables for ease of reference.

TABLE III.
PEAK TEMPERATURE OF SLOT VIAS TYPES

		SLOT VIAS		
	No Via	**Au Lined Via**	**Via cavity**	**Au-filled**
GaAs: 1 W/mm	156 °C	151 °C	173 °C	128 °C
GaN-on-Si: 3.6W/mm	208 °C	211 °C	217 °C	198 °C
GaN-on-SiC: 3.6W/mm	206 °C	213 °C	218 °C	201 °C

For this set of cases we begin to see some interesting trends emerge. First, it is clear that the substrate material clearly matters for these cases. Introducing slot vias with limited no sidewall metallization (the via-cavity case) for GaN-on-SiC results in a penalty of a 12°C increase in peak temperature as compared to the baseline case, while the nominally lined case results in a somewhat lower 7°C penalty. In the other extreme, filling these same via structures reduces the peak temperature by just 5°C relative to the baseline case – an improvement that likely does not merit the added cost and complexity of such an approach. What is implied is a benefit one can realize in choosing or developing a process that enables a thicker, well controlled liner metallization. GaN-on-Si exhibits a similar response across the various cases where filling the slot vias results in a peak temperature reduction of 11°C. The lowest thermal conductivity substrate case (GaAs) exhibit the most profound impact for the slot via cases. The lined slot via case by contrast to previous substrates actually exhibits a slight reduction in peak temperature over the baseline case, whereas the hypothetical air cavity case results in a 22°C rise over the lined case – a clear indication that control of back metallization processes is crucial for devices comprising such substrates. And the Au-fill case exhibits a significant improvement in comparison with the no-via case – a reduction of 28°C - an illustration that such a via configurations can serve to significantly enhance thermal performance of similar GaAs devices. These results make sense when considering that slot-vias are in close proximity to the device active area and hence fall within regions of significant heat transport or spreading. The relative thermal conductivities of gold in comparison with that of the various substrate materials also explains why the effect is far more profound on the GaAs devices.

The last via type explored in this investigation is the segmented slot-type. For this via type, some foundries place design rule restrictions on the dimensions of their through-substrate vias due to process constraints or concerns with reliability. And often this restriction comes in the form of a "one size only" constraint. Therefore designers often adopt a strategy of lining-up several such structures in a single source contact pad to keep the overall lead inductance low. As mentioned earlier, we chose a fixed dimension of 30 x 60 μm^2 for the via type in this comparative study and fitted two such structures in each source region 140 μm apart edge to edge. Table IV summarizes the results for our simulations of segmented via types across substrate and fill types.

TABLE IV.
PEAK TEMPERATURE OF SEGMENTED SLOT VIA TYPES

		SEGMENTED 30x60 μm SLOT VIAS		
	No Via	**Au Lined Via**	**Via cavity**	**Au-filled**
GaAs: 1 W/mm	156 °C	153 °C	159 °C	144 °C
GaN-on-Si: 3.6W/mm	208 °C	209 °C	209 °C	205 °C
GaN-on-SiC: 3.6W/mm	206 °C	207 °C	208 °C	204 °C

What is observed is that segmenting slot vias provides a means of achieving low ground inductance with little to no thermal penalty for the cases studied here. In fact, the GaN-on-Si and GaN-on-SiC cases in this comparative study exhibit essentially no thermal impact across all fill-types. This is not surprising given that the volume immediately below the source contacts looks essentially like that of the baseline case immediately about the centerline subdividing unit gate width - the region of highest temperature. It also suggests that this strategy, while effective for this specific case, may require further simulation and optimization for

other layouts. Of particular concern would be devices of shorter unit gate width or the placement of vias in proximity to regions of peak temperature gradient.

For the lower thermal conductivity GaAs substrate cases, the improvement associated with lined vias is also of limited benefit, an improvement of just 3°C. However, filling the via provides a 12°C improvement as compared to the baseline case.

As we have shown, the thermal impact of establishing a filled-via approach is minimal for higher thermal conductivity substrate materials. For the cases studied here, the added cost and complexity of such processes are in many cases likely difficult to justify. As we have shown, for the lower thermal conductivity GaAs substrate material the approach is more compelling, but needs to be considered among a range of other device design options such as the via segmentation approach presented here, increasing gate-to-gate pitch or optimization of other thermally limiting factors such as the attach process. For example, we have shown by simulation that decreasing average AuSn bond line thickness by such means as deposited backside eutectic can impact overall thermal performance by amounts similar to some of the effects described previously in this work. As an example, for the GaN-on-SiC cases we've shown that reducing the bond line to 12μm results in a peak temperature reduction of ~18°C over the baseline case.

CONCLUSION

For the device structures covered in this comparative study, it has been shown that end-vias exhibit no significant impact on the thermal performance of the transistor studied irrespective of the materials systems or fill-type. For the relatively low thermal conductivity GaAs substrate cases, slot-vias and the segmented slot-via variant have been shown to require careful control of the gold metallization process and metal fill of such structures can provide significant thermal benefit depending on device layout. As discussed, the cost and complexity of the latter approach has to be weighed against that of other process and design approaches that can realize benefits of similar order. For the higher thermal conductivity materials systems such as GaN-on-Si and GaN-on-SiC, process control of via lining is shown to be less critical and filling slot-vias is of clear questionable benefit. Pursuing a segmented slot via strategy can be a more effective way of managing peak temperatures in these materials, but the specifics of the implementation need to be considered.

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ACRONYMS

GaAs: Gallium Arsenide
ISV: Individual Source Via
CMC: Copper-Molybdenum-Copper
Au: Gold
SiN: Silicon Nitride
Cu: Copper
AuSn: Gold-Tin Eutectic solder
IR: Infra-red