Threshold Voltage Extraction Method for 2D Devices with Power-law μ(n_S) Dependence

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Abstract

A new method for the extraction of the threshold voltage in Field-Effect-Transistors is presented. It is suited for all classes of devices whose mobility exhibits a power-law dependence on carrier concentration. The extracted threshold voltage V_T has a physical meaning: the sheet carrier concentration is proportional to V_G-V_T, as was shown using Hall studies in companion gated Hall devices.

INTRODUCTION

Threshold voltage is with transconductance one of the most fundamental parameters characterizing a Field-Effect-Transistor (FET). It roughly corresponds to the gate voltage above which the drain-source current I_{DS} becomes appreciable and the $I_{DS}(V_G)$ characteristics becomes more or less linear. However, due in particular to the fact that the constraints for various needs such as modeling, technology characterization or production assessment are not the same, there is no generally accepted unique definition of V_T.

Among the profusion of definitions used in the literature [1], many are phenomenological: the "threshold voltage" may correspond to the gate voltage for a given small I_{DS} current value, or be the intercept at I_{DS}=0 of the extrapolation of a linear region in the $I_{DS}(V_G)$ characteristics, or of the transconductance $g_m(V_G)$ characteristics, etc…

A more physical method is the ratio method [2-5], based on the assumption that the inverse mobility has a linear variation as a function of the carrier channel density $^1 = {}_0{}^1 \times (1 + (V_G \quad V_T))$. Based on this assumption, it can be shown that the ratio $I_{DS} / \sqrt{g_m}$ (sometimes termed the Y-function) should be proportional to $V_G \quad V_T$, and should not depend on the mobility variation parameter [2], nor on the drain and source series access resistance [3].

However, this procedure doesn't provide reliable results when the assumption on the mobility fails. This is notably the case for a variety of devices and technologies, for which the mobility dependence on the channel sheet carrier concentration is fairly well described using a power-law behavior: $\mu \, n_S$. In compound semiconductor devices, this was observed e.g. in low density GaN/AlGaN/GaN heterostructures [6] or high-mobility InSb/InAlSb heterostructures [7]. Fig.1 shows the mobility behavior $\mu \, n_S^{0.74}$ measured in Hall devices made using AlGaAs/ GaInAs/GaAs pseudomorphic structures. Moreover, this behavior is also common in non-III-V devices, such as polycrystalline silicon based Thin-Film-Transistors (TFT) [8], or organic transistors such as oligothiophene TFT [9].

We propose a new simple and robust method for the determination of the threshold voltage in FETs with power-law $\mu \, n_S$ dependence valid in some range above threshold. The resulting threshold value is independent of parasitic series resistances such as the drain and source access resistance, and of course of the mobility variation.

This physically based method is illustrated using experimental results from pHEMT transistors. The threshold voltage V_T extracted from these measurements compares well with the value obtained from the dependence of the sheet electron density $n_s(V_G)\mu\,(V_G \quad V_T)$, that is measured through Hall measurements in pHEMT like gated Hall devices fabricated in the same wafers.

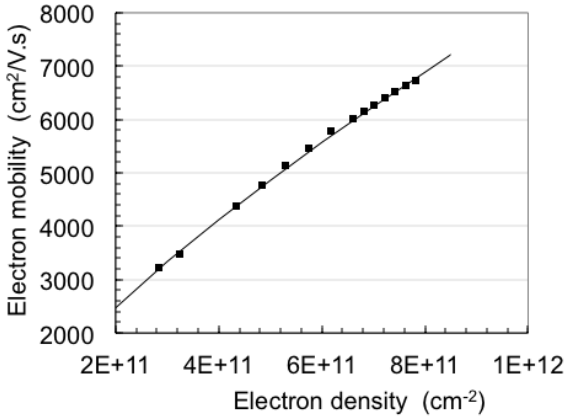

Fig.1 Mobility dependence on the channel electron density measured using a Hall cross shaped AlGaAs/InGaAs/GaAs pHEMT with a gate all over the channel (see Fig.3). The mobility shows a power-law dependence on the electron density, with exponent determined to be α=0.74.

THRESHOLD VOLTAGE EXTRACTION

In III-V based FETs, there is a small ungated region in series with the gated channel between the source and drain contacts, as shown in the schematic view of a heterostructure based FET in Fig.2. Using a standard approach derived from the archetypal long-channel MOSFET 1D approximation [10], it can be shown that, at least for low drain-source bias when the channel electrons are in the mobility regime,

the drain-source current is related to the channel potential at points y_1 and y_2 (Fig.2) through:

$$I_{DS} = \frac{W}{L_G} \times \mu_n \times C_0 \times \left(V_G - V_T - \frac{V_1 + V_2}{2} \right) \times (V_2 - V_1) \quad (1)$$

In (1), C_0 is essentially the gate-channel specific capacitance, $L_G = y_2 - y_1$ is the gate length, W is the channel width, and $V_1 = V(y_1)$ and $V_2 = V(y_2)$ are respectively the channel potential at the abscissae y_1 and y_2 in the channel (Fig.2).

Denoting V_S and V_D the potentials imposed externally to the source and drain contacts, one has:

$$V_1 = V_S + R_{acc} I_{DS} \text{ and } V_2 = V_D - R_{acc} I_{DS}, \quad (2)$$

where the access resistance R_{acc} is the sum of the drain or source ohmic contact resistance in series with the resistance of the associated ungated portion of the channel. Inserting (2) in (1), one gets after trivial manipulation

$$I_{DS} = \frac{\frac{W}{L_G} \times \mu_n \times C_0 \times \left(V_G - V_T - \frac{V_{DS}}{2} \right) \times V_{DS}}{1 + 2R_{acc} \times \frac{W}{L_G} \times \mu_n \times C_0 \times \left(V_G - V_T - \frac{V_{DS}}{2} \right)}, \quad (3)$$

which is identical to the general expression of the drain-source current I_{DS} in a silicon MOSFET when the access resistances are taken into account [3]. The electron density $n_S(y)$ is very slightly modulated due to the voltage drop along the channel, its mean value is related to the gate and drain bias through:

$$n_S = \frac{C_0}{e} \left(V_G - V_T - V_{DS}/2 \right). \quad (4)$$

The mobility dependence on n_S, or equivalently on V_G,

$$\mu_n = \mu_{n0} \times \frac{n_S}{n_{S0}} \text{ or } \mu_n = \mu_{n0} \frac{\left(V_G - V_T - V_{DS}/2 \right)}{\left(V_{G0} - V_T - V_{DS}/2 \right)} \quad (5)$$

valid for any arbitrary (μ_{n0} , n_{S0}) conditions, is injected in (3) before calculating the total channel resistance $R = V_{DS}/I_{DS}$:

$$R = 2R_{acc} + K \times \left(V_G - V_T - V_{DS}/2 \right)^{(1+\alpha)} \quad (6)$$

where the coefficient K stands for the expression:

$$K = \frac{L_G}{W} \times \frac{1}{\mu_{n0} \times C_0} \left(V_{G0} - V_T - V_{DS}/2 \right)^{-\alpha}. \quad (7)$$

The first derivative wrt. V_G of the channel resistance reads:

$$R' = \frac{dR}{dV_G} = (1+\alpha) K \times \left(V_G - V_T - V_{DS}/2 \right)^{(2+\alpha)} \quad (8)$$

and its 2nd derivative is:

$$R'' = \frac{d^2R}{dV_G^2} = (1+\alpha)(2+\alpha) K \times \left(V_G - V_T - V_{DS}/2 \right)^{(3+\alpha)} \quad (9)$$

Finally, it turns out that the ratio $-R'/R''$ is expected to depend on V_G in a linear way, without any dependence on the various device parameters introduced in (3):

$$\frac{R'}{R''} = \frac{1}{2+\alpha} \times V_G - V_T - \frac{V_{DS}}{2}, \quad (10)$$

Thus, the $-R'/R''$ against V_G graph should be a straight line intercepting the x-axis at V_T-V_{DS}/2, and whose slope is directly related to α, the exponent in the mobility expression.

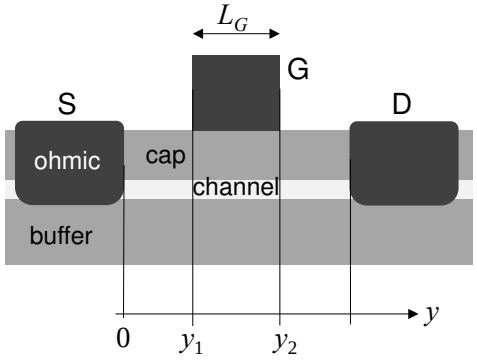

Fig.2 Schematic view of the cross-section of a heterostructure based FET, with definition of the points y_1 and y_1 along the channel.

The –R'/R'' ratio vs. V_G can be easily computed from a discrete $I_{DS}(V_G)$ characteristics taken at equally spaced points V_{G_n} with $V_{G_{n+1}} - V_{G_n} = \Delta V_G$. From the Taylor expansion:

$$R_{n\pm1} \approx R_n \pm R'_n \Delta V_G + R''_n \Delta V_G^2/2 \quad (11)$$

the ratio can be computed as:

$$\left. \frac{R'}{R''} \right|_n = \frac{(R_{n-1} - R_{n+1})}{R_{n+1} - 2R_n + R_{n-1}} \cdot \frac{\Delta V_G}{2}. \quad (12)$$

In the subthreshold region, the free carrier density depends exponentially on V_G, and hence the subthreshold drain-source current reads:

$$I_{DS} \propto \exp \frac{V_G - V_T}{\lambda kT} \quad (13)$$

where λ denotes some capacitance ratio [11], larger than 1 depending on the kind of FET. With the same definitions as before, one can easily check that:

$$R_{n\pm1} = \exp(\mp \frac{\Delta V_G}{\lambda kT}) R_n, \quad (14)$$

and the value of–R'/R'' computed according to (12) reads:

$$\left. \frac{R'}{R''} \right|_n = \frac{V_G}{2} \cdot \coth \frac{V_G}{2 \lambda kT} \quad (15)$$

The –R'/R'' plot tends towards a constant for $V_G < V_T$, which is approximately equal to $V_G/2$ as soon as $V_G > 2 \lambda kT$.

EXPERIMENTAL

The devices used in this study are based on AlGaAs/InGaAs/GaAs pseudomorphic heterostructures on a semi-insulating substrate, designed for the manufacturing of high-sensitivity Hall effect devices with excellent metrological performances [12]. Wafers were grown by various providers, using MBE. The QW channel mainly consists of a 10 or 13 nm thick $In_yGa_{1-y}As$ layer with In content y amounting to 15% or 20%, depending on the wafers. Free electrons in the channel are provided by a delta doping layer in the x≈30% $Al_xGa_{1-x}As$ cap layer. Doping

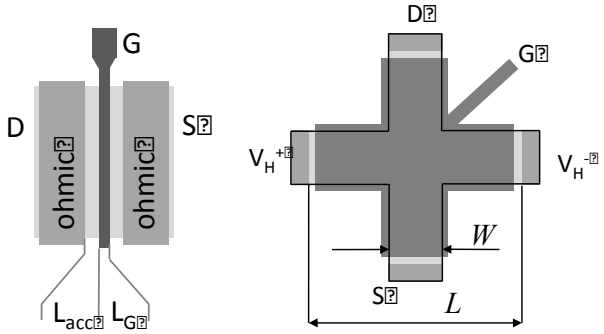

Fig.3. Schematic view of the devices used in this study. Left: normally-on FET, with access length L_{acc} on each side of the gated region and gate length L_G. Right: Gated Hall device. Channel length L=200 µm, arm width W=50 µm.

density was chosen to get an n_S=6.5 to 9x10^{11}cm^{-2} electron density. The cap layer L_A is rather thick, between 100 nm and 260 nm, depending on the wafers. In this case, the gate-channel capacitance is essentially due the cap layer thickness $C_0 \quad _S / L_A$, with low influence of the capacitance due to the finite 2D density-of-states in the quantum well, or from other quantum effects.

From these wafers, two kinds of devices were fabricated. For the transistor studies, several series of normally-on pHEMT as depicted in Fig.3 were designed using optical lithography. The gate length L_G was varied between 1 and 15 µm. The ungated access length L_{acc} between each drain or source region and the gated portion of the channel was varied between 1.5 and 3 µm. The channel width is comprised between 10 and 100 µm. Typical $I_{DS}(V_G)$ results are shown in Fig.4.

For the Hall effect measurements, Greek-cross shaped Hall effect devices were designed (Fig.3), with a gate covering almost the entire active region between contacts. Thus, the electron density remains homogenous when varying the gate voltage, at least as long as the ohmic voltage drop in the sample, remains small.

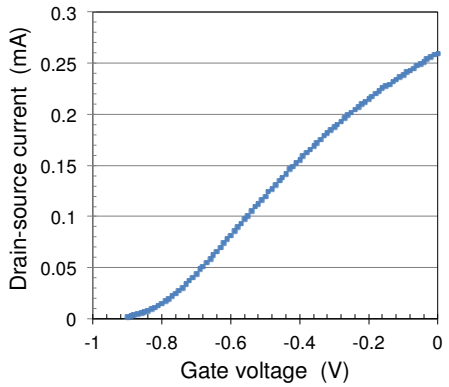

Fig.4 $I_{DS}(V_G)$ characteristics of a jumbo pHEMT transistor with 2 µm gate length and 2 µm access length between ohmic contact and gate. Cap layer thickness is about 110 nm.

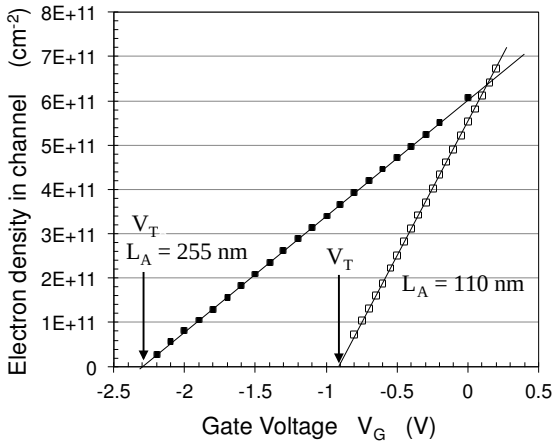

Fig.5 Experimental dependence of the Hall electron density in Hall cross-shaped AlGaAs/InGaAs/GaAs pHEMT-like Hall devices with cap layer thickness 110 and 255 nm. The electron density increases proportionally with the V_G increase, unambiguously defining a threshold voltage V_T.

In order to remain within Van der Pauw conditions [13], and thus to allow for precise Hall measurements, we took several precautions. The complete gate covering ensures that the electron density remains homogenous for every gate voltage value. The Greek crosses have a L/W=4 geometry in order to avoid shunting by the lateral electrodes. Indeed, under such conditions, the geometrical factor G_H in the Hall voltage [13] is practically equal to unity [14]. Finally, the $V_H(V_G)$ characteristics were measured using a constant low bias voltage V_{in} equal to 20 mV, the bias current I_{in} was measured and used in (16) to calculate n_S.

Moreover, in a degenerate QW Hall, the scattering factor r_H can be assumed to be unity too.

Thus, measuring the Hall voltage:

$$V_H = \frac{G_H \times r_H}{en_s} I_{in} B \qquad \frac{1}{en_s} I_{in} B \qquad (16)$$

allows for an accurate determination of the sheet carrier density as a function of V_G. Combining it with sheet resistivity $R_{sq}(V_G)$ obtained from standard Van der Pauw resistivity measurements as a function of the gate voltage yields

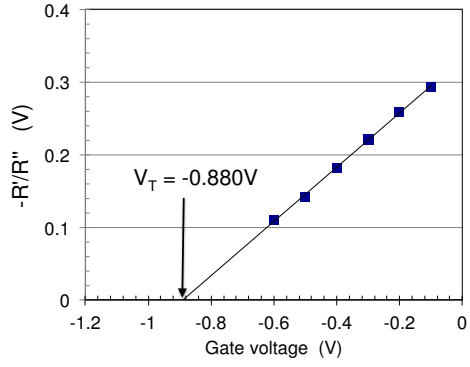

Fig.6 Ratio $-R'/R''$ calculated by applying Eq.(12) to the $I_{DS}(V_G)$ data of Fig.4, for ΔV_G=100 mV. The ratio shows a linear dependence on V_G-V_T. The threshold voltage is very close to that determined by Hall measurements in Hall devices from the same wafer.

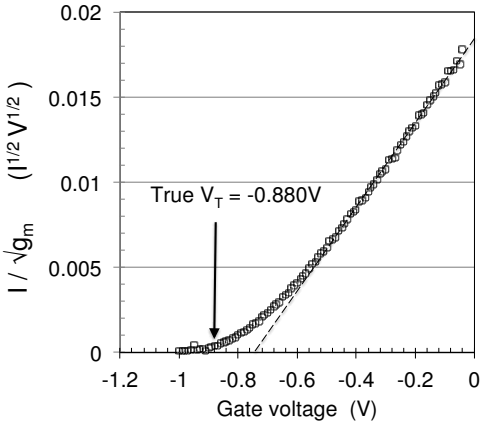

Fig.7 Standard $I_{DS}/\sqrt{g_m}$ ratio method applied to the $I_{DS}(V_G)$ data of Fig.4. The curvature of the curve renders the extraction of a threshold voltage more difficult. The intercept of the dashed curve is more than 150mV apart from the true threshold voltage.

the mobility dependence $\mu_n(V_G)$ or $\mu_n(n_S)$ shown in Fig.1. The linear behavior of $n_S(V_G)$ is shown in Fig.5 for two devices with cap layer thickness 100nm and 260 nm.

THRESHOLD VOLTAGE EXTRACTION – DISCUSSION

The quantity –R'/R" obtained using Eq.(12) from the $I_{DS}(V_G)$ data of Fig.4. is perfectly linear (Fig.6). The determined V_T =-880 mV fits closely with the Hall $n_S(V_G)$ value, -900 mV. Note that the devices were 6 mm from each other. On the contrary, the standard $I_{DS}/\sqrt{g_m}$ ratio method lacks linearity and yields a value different by more than 150 mV (Fig.7). Fig.8 shows the robustness of the method. The V_T values obtained by choosing 3 different V_G increments of 0.2, 0.4 and 0.6 V perfectly coincide. The asymptotes at $V_G/2$ for $V_G < V_T$ are in agreement with Eq.(15). Fig.8 also suggests that just a few widely spaced $I_{DS}(V_G)$ points above threshold are sufficient to get a precise determination of V_T, thus limiting the effect of noise in the procedure.

CONCLUSION

A new physical model, valid in the case of mobility with power-law dependence on the sheet carrier density, has been proposed for the extraction of the threshold voltage in FETs. It relies on the calculation of the –R'/R" quantity from a few $I_{DS}(V_G)$ data above threshold. The result is independent of the mobility variation and series resistance. This model has been tested and validated up to now for AlGaAs/InGaAs/GaAs devices with a rather thick cap layer (≈100 nm). Owing to the fact that it provides a threshold voltage value with clear physical meaning, it would be interesting to check whether it also holds for other kinds of devices. When performing coupled field-effect transistor and Hall measurements, care should be taken to design Hall devices with negligible short-circuit current [11] in the lateral contacts.

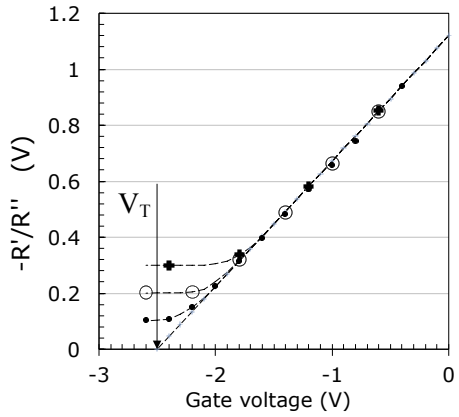

Fig.8 Ratio $-R'/R"$ for a transistor with large cap layer (258 nm), calculated for different values of the V_G increment. ΔV_G is respectively equal to 200 (small dots), 400 (large hollow dots) and 600 mV (thick crosses). The curves show a linear dependence on V_G-V_T for large enough V_G, and an asymptotic behavior –R'/R" → $\Delta V_G/2$ below and around V_T.

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REFERENCES

[1] A. Ortiz-Conde, F.J. García Sánchez, J.J. Liou, A. Cerdeira, M. Estrada, Y. Yue, Microelectronics Reliability 42, 583–596 (2002)
[2] G. Ghibaudo, Electron. Lett, 24, 543-545 (1988)
[3] S. Jain, IEE Proc., Part I: Solid-State Electron Dev. 135, 162-164 (1988)
[4] W. Fikry, G. Ghibaudo, H. Haddara, S. Cristoloveanu, M. Dutoit, Electron. Lett. 31, No.2, 762-764 (1995)
[5] P.K. McLarty, S. Cristoloveanu, O. Faynot, V. Misra, J.R. Hauser, J.J. Wortman, Solid-State Electronics 38, 1175-1177 (1995)
[6] M.J. Manfra, K.W. Baldwin, A.M. Sergent, R.J. Molnar and J. Caissie, Appl. Phys. Lett. 85, 1722-1724 (2004)
[7] A.M. Gilbertson, W.R. Branford, M. Fearn, L. Buckle, P.D. Buckle, T. Ashley, and L.F. Cohen, Phys. Rev. B79, 235333 (2009)
[8] Mark D. Jacunski, Michael S. Shur, and Michael Hack, IEEE Trans. Electron Dev.43, 1433-1440 (1996)
[9] G. Horowitz, M.E. Hajlaoui, and R. Hajlaoui, J. Appl. Phys. 87, 4456-4463 (2000)
[10] S.M. Sze and K.K Ng, *Physics of semiconductor devices*, 3rd ed., John Wiley & Sons (2006).
[11] R.J. van Overstraeten, G.J. Declerck, P.A. Muls, IEEE Trans. Electron Dev., 22, 282-288 (1975).
[12] V. Mosser, A. Kerlain, Y. Haddab, R. Morton and M.J. Brophy, *Ensuring high yield and good reliability for mass-produced high-performance Hall effect sensors*, 2006 GaAs ManTech Technical Digest, Vancouver, BC, Canada, pp. 291-294, April 2006.
[13] R.S. Popovic, "*Hall Effect Devices*", 2nd ed., IOP Publishing, Bristol and Philadelphia, 2004.
[14] J. Przybytek, V. Mosser and Y. Haddab, *LF noise in cross Hall effect devices -geometrical study*, Proc. SPIE Vol. 5113, 475-483, May 2003

ACRONYMS

FET:	Field Effect Transistor
MBE:	Molecular Beam Epitaxy
pHEMT:	Pseudomorphic High Electron Mobility Transistor
QW:	Quantum Well