InAlN/GaN HEMTs With Over 100-GHz f_T Using an Improved Y-Gate Process by an i-Line Stepper

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Abstract

We previously developed a Y-gate process with a conventional i-line stepper. The process enabled us to obtain a current gain cutoff frequency (f_T) of 70 GHz for InAlN/GaN high electron mobility transistors (HEMTs). In this study, we reduced both gate length (L_g) and over-gate length (L_{og}) to decrease gate-source capacitance (C_{gs}). We obtained a remarkably short L_g of 100 nm, with an i-line stepper process. Short L_{og} of 340 nm was also obtained. InAlN/GaN HEMTs were fabricated with this improved process realizing a C_{gs} reduction of 36% compared to the previous process. As a result, f_T over 100 GHz was successfully achieved. This simple and low C_{gs} process is suitable for low cost production of high speed InAlN/GaN HEMTs.

INTRODUCTION

High-speed operations of a current gain cutoff frequency (f_T) over 100 GHz have been reported for InAlN/GaN high electron mobility transistors (HEMTs) with gate length (L_g) less than 100 nm [1–3]. However, complicated processes such as an electron beam lithography and a regrowth technology were necessary. Therefore, we have focused on low cost and simple technologies suitable for mass production. We previously demonstrated a 150-nm Y-gate process with a conventional i-line stepper [4]. The process enabled us to obtain f_T of 70 GHz for InAlN/GaN HEMTs. To achieve higher f_T, we tried to optimize the Y-gate process to decrease gate-source capacitance (C_{gs}) by reduction of L_g and over-gate length (L_{og}).

In this paper, we describe epi structures and the detail of the Y-gate process. Then, we show the characterization data of InAlN/GaN HEMTs fabricated with this new process.

EPI STRUCTURES

InAlN/GaN HEMT epitaxial layers were grown by metal-organic chemical vapor deposition (MOCVD), on 100 mm high-resistance silicon substrates. The typical structure consists of an AlGaN buffer layer, a GaN buffer layer, an AlN interlayer and a lattice-matched InAlN barrier layer. Sheet resistance is approximately 280 Ω/sq.

A GaN cap layer is effective to reduce the gate leakage current (I_g) which is a major issue of InAlN/GaN HEMTs [5-6]. In our previous study, we demonstrated sufficiently

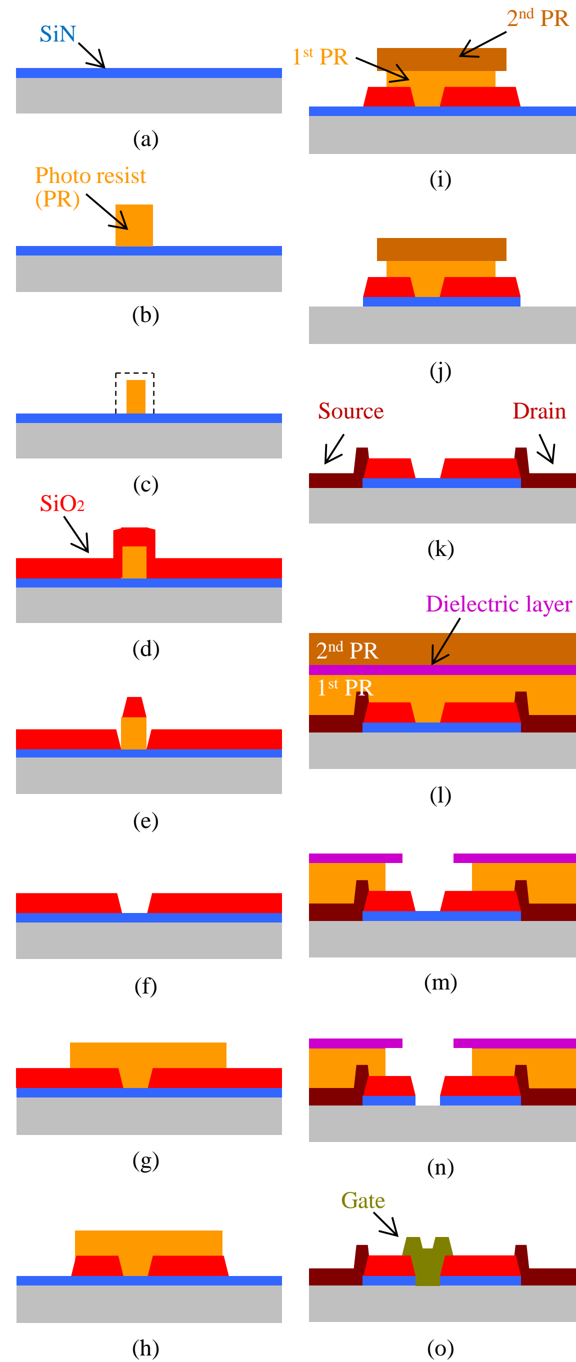

Fig. 1 Y-gate process flow.

11

low I_g of 1.6×10^{-6} A/mm, by introducing the GaN cap layer [4]. However, introduction of the GaN cap layer sacrifices high transconductance (g_m). We have developed a new epitaxial growth technique which can maintain a low I_g without the GaN cap layer. In this study, we used this non-GaN cap layer structure.

Y-GATE PROCESS

An overview of the Y-gate process flow is shown in Fig. 1. First of all, a sputtered SiN film was deposited on the surface by using an electron cyclotron resonance plasma. This deposition method can create denser films than those of conventional plasma-enhanced chemical vapor deposition (PECVD) methods. The refractive index and the thickness of the SiN film were 2.05 and 40 nm, respectively. Then, a photo resist (PR) pattern with 1.0-µm-thick and 270-nm-width was obtained by an i-line stepper. In order to obtain the precise gate length, the shape of the resist pattern shall be as rectangular as possible. The PR pattern was shrunk by an O_2 plasma. Next a 300-nm-thick SiO_2 film was deposited on the pattern by sputtering. The SiO_2 film adhering to the sidewall of the PR was removed by a buffered hydrofluoric acid (BHF) solution. Then the PR was lifted off. In the previous process, L_g after this reverse gate process was 120 nm. After optimization of the PR shrinkage process, we could obtain L_g of 70 nm.

To fabricate the ohmic contacts, a SiO_2 and SiN film stack needed to be removed. The SiO_2 film is 300 nm thick, so a multi-step process of reactive ion etching (RIE) and buffered hydrofluoric acid (BHF) is required. The first 150 nm of film is removed by a high-power Cl_2/BCl_3 RIE process. The RIE process then switches to a low power step to etch another 100 nm of SiO_2. Finally, to clear the final remaining SiO_2 layer, a BHF solution was employed in order to minimize surface damage. Additionally, the selectivity of SiO_2 to SiN in BHF is 100:1, so the SiN acts as an etch stop. The ohmic contact formation process continues with a two-step photo process that is optimized for metal lift-off and is shown in Fig. 1, step (i). An additional PR layer is added to an existing one which creates an undercut profile. The last step in ohmic contact formation is to etch the SiN film in a RIE tool using CF_4. Subsequently, source and drain contacts are formed on the InAlN barrier layer through a deposition and lift-off process, followed by a rapid thermal anneal and is shown in Fig. 1, steps (j-k).

Figure 1, steps (l-o), outline the gate module. The gate formation consists of three different layers which were introduced to reduce L_{og}. This module starts with a dielectric layer sandwiched between a first and second PR layer, shown in Fig. 1, step (l). We have found that the gate opening is smaller with a three layer stack rather than a two layer. The SiN at the base of the gate region is etched with CF_4 RIE and is shown in Fig. 1, step (n). The dielectric layer acts as a mask in the gate deposition, which allows for a nice profile and also helps with evaporated metal lift-off.

A transmission electron micrograph (TEM) image of the

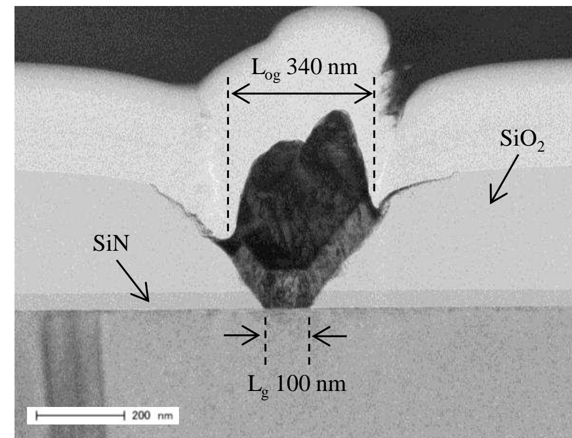

Fig. 2 Cross-sectional TEM image.

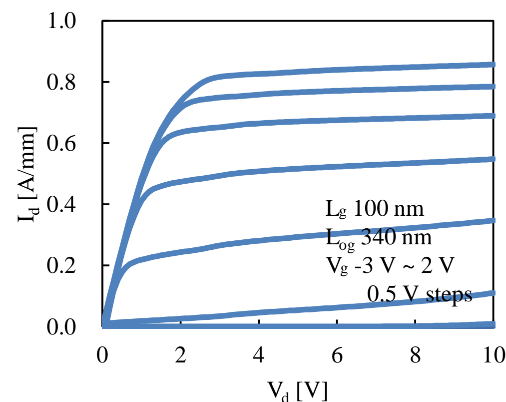

Fig. 3 Drain characteristics.

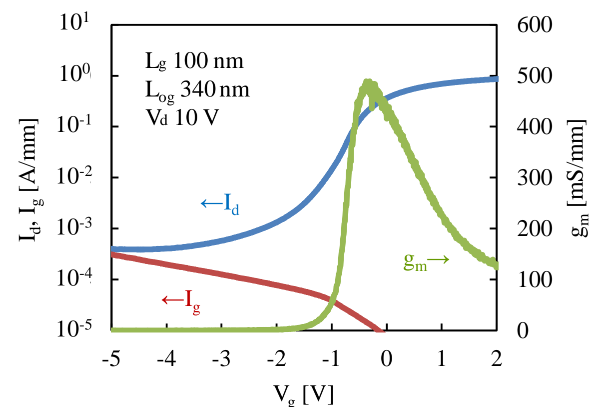

Fig. 4 Transfer characteristics.

cross section of the InAlN/GaN HEMT is shown in Fig. 2. L_g was 100 nm (150 nm in the previous process). L_g is a little longer than that after the reverse gate process because L_g is enlarged at the final SiN etching (Fig.1, step (n)). L_{og} was 340 nm without tail (600 nm in the previous process). We confirmed both L_g and L_{og} were successfully reduced. The gate sidewall was tapered and its angle was approximately

60º. We can control this angle by changing the SiO_2-thickness and RIE conditions. The angle is important, since it determines the parasitic gate capacitance and the electric field at the gate edge.

EVALUATION

We measured the DC characteristics of the InAlN/GaN HEMTs fabricated with the improved Y-gate process. The drain characteristics are shown in Fig. 3. The evaluated deice has L_g of 100 nm, L_{og} of 340 nm and gate width (W_g) of 80 × 1 μm. The gate voltage (V_g) was swept from -3 to 2 V with 0.5 V steps. Maximum drain current (I_d) of 0.86 A/mm was observed. Even if InAlN barrier was applied, maximum I_d was relatively low because of thin barrier and high contact resistance. The on-resistance extracted at V_g of 2 V and drain voltage (V_d) in the range between 0 and 1.0 V was 1.8 Ωmm. Next, the transfer characteristics were measured at V_d of 10 V as shown in Fig. 4. Though the GaN cap was not applied, I_g of 7.7×10^{-5} A/mm at V_g of -2V was obtained. The peak g_m was as high as 490 mS/mm.

We measured the S-parameters using an Agilent 8510C network analyzer for the InAlN/GaN HEMTs with W_g of 50 × 2 μm from 10 to 80 GHz. After the pad parasitic was de-embedded, we extracted C_{gs} and g_m from an equivalent circuit model obtained from the measured S-parameters. L_g and L_{og} dependence of C_{gs} and g_m are shown in Fig 5. The highest g_m of 490 mS/mm was achieved at L_g of 220 nm. Short L_g is effective in reduction of C_{gs} remarkably. On the other hand, short L_{og} is also effective in reduction of C_{gs}. The lowest C_{gs} of 0.58 pF/mm was obtained at L_g of 100 nm and L_{og} of 340 nm. Since C_{gs} in the previous process was 0.90 pF/mm, we could reduce C_{gs} by 36%.

The gain characteristics are shown in Fig. 6. f_T of 110 GHz and maximum oscillation frequency (f_{max}) of 140 GHz were obtained under the bias condition of V_d of 10 V and I_d of 300 mA/mm. We could achieve over 100 GHz f_T, however, the f_{max} / f_T ratio was as low as 1.3. The reason for such low ratio is the high gate resistance because both L_{og} is short and electrolytic plating process is not applied. We could believe much higher f_{max} shall be achieved by introduction of the electrolytic plating process.

CONCLUSIONS

We successfully improved the Y-gate process with C_{gs} reduction of 36% compared to the previous process. As a result, f_T over 100 GHz was achieved. This simple process with a conventional i-line stepper is suitable for low cost production of high speed InAlN/GaN HEMTs.

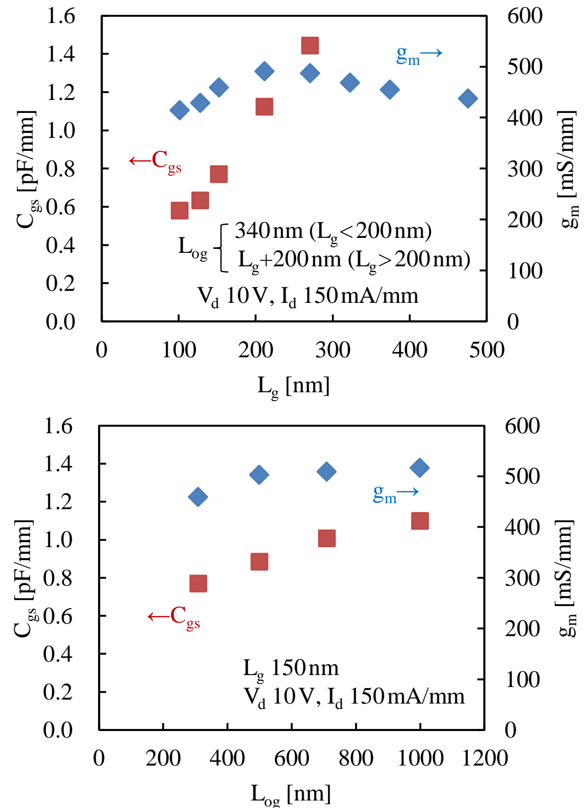

Fig. 5 L_g and L_{og} dependence of C_{gs} and g_m.

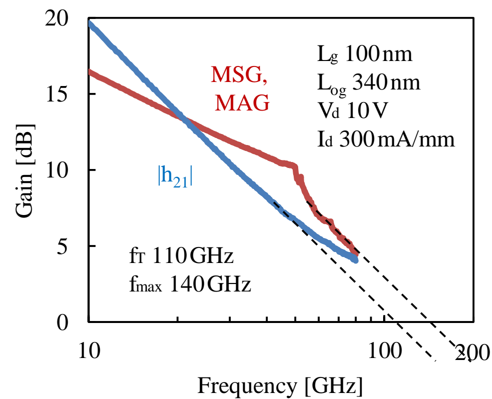

Fig. 6 Gain characteristics.

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ACRONYMS

HEMT: High Electron Mobility Transistor
I_g: Gate Leakage Current
RIE: Reactive Ion Etching