A CMOS-Compatible Fabrication Process for Scaled Self-Aligned InGaAs MOSFETs

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KEYWORDS: MOSFETs, CMOS process, Self-aligned, III-V dry etch, digital etch

Abstract

We have developed a scalable gate-last process to fabricate planar self-aligned InGaAs Quantum-well (QW) MOSFETs that relies on extensive use of dry recess. The fabrication sequence yields precise control of all critical transistor dimensions, in particular, the length and thickness of the channel and the access regions. The process involves a combination of anisotropic and isotropic F-based dry etching of refractory metal ohmic contacts that are formed early in the process. Anisotropic Cl-based dry etching is used to recess the In-based III-V cap material. A digital etch technique that achieves a thickness control down to ~1 nm is used to trim the channel to its final thickness. We have demonstrated L_g=20 nm MOSFETs with 15 nm contact-gate separation and good electrical characteristics. A device design optimized for transport exhibits a record transconductance of 3.1 mS/µm.

INTRODUCTION

InGaAs is a promising candidate for n-type channel material for future CMOS due to its superior electron transport properties [1]. Several self-aligned device architectures have been demonstrated, such as the recessed-gate [2-5], implanted source and drain (SD) [6-7], regrown SD [8-9] and alloyed Ni-InGaAs contacts [10-11]. Among these, the recessed-gate technology is an attractive option due to its scalability and simplicity. It has also yielded outstanding performance results [4-5]. This paper describes in detail a self-aligned recessed-gate process for scaled InGaAs QW-MOSFETs that emphasizes scalability, performance and manufacturability by making extensive use of dry etching and Si-compatible materials.

DEVICE FABRICATION OVERVIEW

A prototypical starting heterostructure used in our work is sketched in Fig. 1a [3]. On an InP substrate, an InAlAs buffer layer is first grown that incorporates a Si δ-doping layer with sheet concentration of $1x10^{12}$ cm^{-2} placed a few nm below the channel. The as-grown channel typically comprises of a composite InGaAs/InAs/InGaAs trilayer. The cap consists of heavily-doped InGaAs, InAlAs and InP layers and the dopant is silicon. Our heterostructures are grown by MBE by IntelliEpi.

Our device fabrication process integrates a number of features developed in our group over the last few years [2-5]. The key steps are illustrated in Fig. 1. The process starts with a W/Mo ohmic contact stack sputtered on the as-grown epitaxial structure (Fig. 1a). This ohmic contact-first approach yields outstanding contact resistance [12]. After E-beam gate patterning, a SiO_2 mask and the W/Mo contact stack are etched by CF_4:H_2 and SF_6:O_2, respectively, anisotropic RIE (Fig. 1b) [3]. Following resist removal, a CF_4:O_2 isotropic RIE is used to laterally undercut the ohmic metal in a controlled manner (Fig. 1c). This is achieved by adding O_2 during RIE [13]. RIE time controls the extent of the lateral recess which eventually sets the final length of the device access regions (L_{access}).

F-based RIE stops at the III-V surface. To recess the III-V cap, anisotropic Cl-based RIE is used. This process is not selective. By calibrating the etch rate, the cap recess can be stopped a few nanometers above the channel (Fig. 1d). At this point, post-RIE damage annealing at 340°C for 15 min is applied to repair the damage introduced in the RIE steps [2].

Beyond this, digital etch (DE) is used to precisely bring the recess to the desired depth [4,14]. This determines the final thickness of the channel (t_{ch}) as well as the thickness of the access region (t_{access}), as shown in Fig. 1e. These two steps are self-limiting [14]. The DE process relies on precisely locating an InAlAs/InP interface that is introduced for this purpose right above the channel and achieves a precision of ~1 nm/cycle. More details of this process are discussed below.

After the last DE cycle, a fresh semiconductor surface is exposed in a final H_2SO_4 cleaning step and this is immediately followed by ALD of 2.5 nm HfO_2 as gate dielectric and Mo gate metal deposition. The HfO_2 is deposited at 250°C and there is no high temperature step after gate dielectric deposition. The device is completed by gate definition, and interconnect via and pad formation as shown in Fig. 1f.

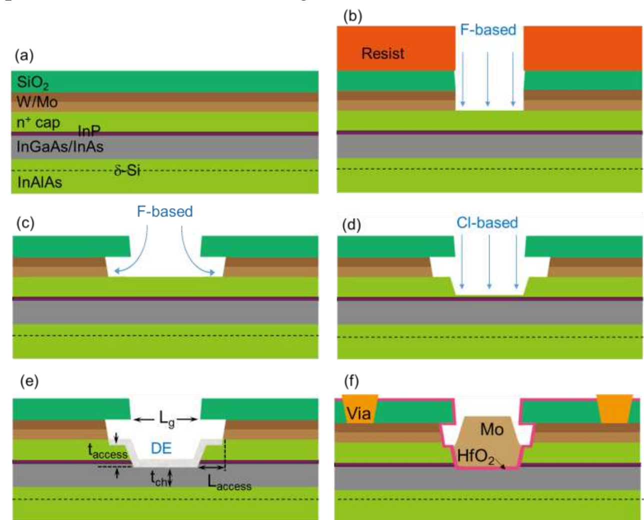

Fig. 1 Illustration of gate recess steps for fabrication of InGaAs QW-MOSFETs. (a) Deposition of ohmic metal and oxide hardmask. (b) Anisotropic SiO_2 and W/Mo etching. (c) W/Mo undercut. (d) III-V cap dry etch. (e) Digital etch. (f) Completed MOSFET.

The entire front-end fabrication (before pad) closely follows the CMOS-compatibility requirements and is completely wet-etch free, lift-off free and Au-free. The overall

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process has a very low thermal budget with the maximum temperature being that of the 340 ºC post-RIE damage annealing. In the next few sections, we describe in more details a few critical process elements.

RIE DAMAGE REMOVAL

From our earlier work, we find that F-based RIE introduces severe damage to the semiconductor structure. A simple 340 ºC post-RIE annealing for 15 min can remove the damage and significantly improves the device characteristics [2].

Fig. 2 shows the capacitance vs. V_g of two finished MOSFETs (a) without post-RIE damage annealing and (b) with post-RIE damage annealing. These devices are fabricated using an earlier version of this process on a simplified heterostructure with unstrained $In_{0.53}Ga_{0.47}As$ quantum-well channel and a 4 nm thick Al_2O_3 gate insulator [2]. The gate length is 20 µm. The capacitance is measured between the gate and the shorted source and drain. The incorporation of damage anneal yields a larger capacitance in the ON-state and lower frequency dispersion around threshold. This is an indication of a reduction in the interface traps density (D_{it}). This is also observed in the subthreshold characteristics of these devices [2]. Unannealed devices exhibit a subthreshold swing of 300 mV/dec, while annealed devices feature 95 mV/dec, a very significant improvement.

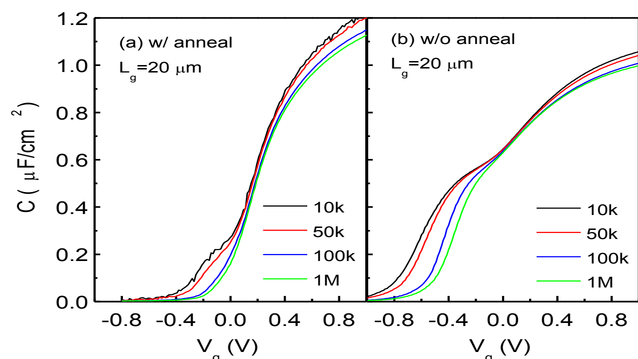

Fig. 2 C-V characteristics for InGaAs MOSFETs with (a), and without (b) the post-RIE damage annealing.

OPTIMIZATION OF III-V DRY ETCH

The III-V dry etch is carried out in a SAMCO RIE-200iP ICP system. The baseline conditions are: gas flow Cl_2:N_2 of 10:3 sccm, pressure of 0.2 Pa, ICP power of 20 W, substrate bias voltage of 130 V, and chuck temperature at 120 ºC. Under these conditions, the etch rate for the composite InGaAs/InAlAs/InP cap is about 0.2 nm/s (Fig. 3). The resulting surface roughness (RMS) is 0.29 nm, slightly rougher than the virgin wafer that featured 0.17 nm (Fig. 4 a,b). The threshold bias for etching is 60 V. A larger bias voltage results in higher etch rate (Fig. 3), but at the expense of increased surface roughness (Fig. 4e). The recipe shows very little temperature dependence for surface roughness (Fig. 4 c,d) and etch rate.

Besides bias voltage, increasing the N_2:Cl_2 gas ratio and the pressure both roughen the surface (Figs. 4 f,g) at a similar etch rate. A BCl_3-based etch recipe similar to [15] was also investigated and discarded due to surface roughening (Fig. 4h).

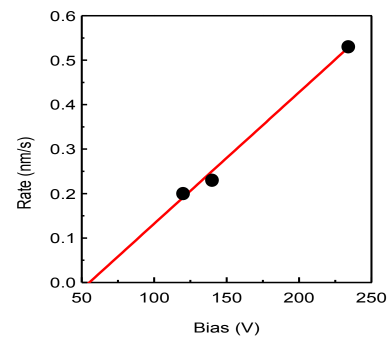

Fig. 3 III-V cap etch rate as a function of substrate bias voltage. Threshold bias voltage for etching is about 60 V.

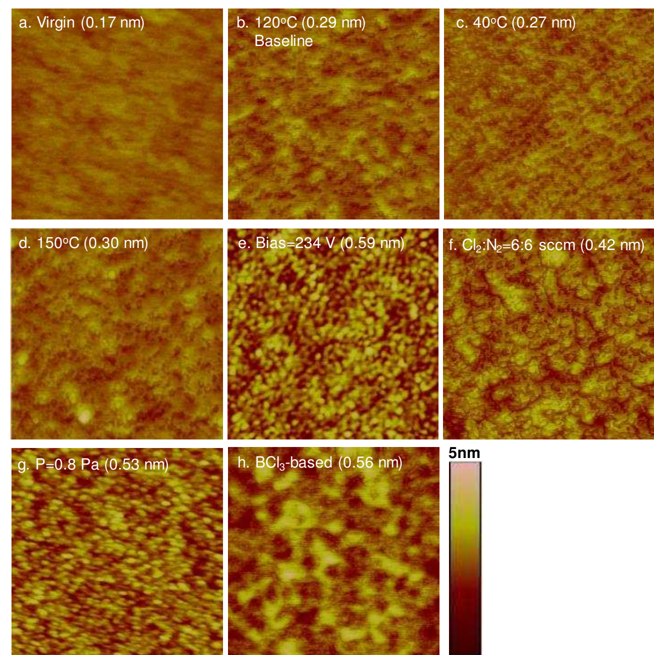

Fig. 4 AFM surface scan for 1 µm^2 area on (a) virgin wafer, (b) dry-etched sample under baseline conditions, (c) 40ºC, (d) 150ºC, (e) increased bias of 234 V, (f) increased N_2:Cl_2 gas ratio, (g) increased pressure and (h) BCl_3-based recipe [15].

The use of high-bias also introduces significant trenching at the two edges of the recess that is caused by ion deflection. Fig. 5 shows cross section SEM images after dry etch using (a) baseline conditions and (b) a high bias condition of 234 V. At the higher substrate bias, significant trenching is evident.

Fig. 6 shows cross-section TEM images of two finished devices etched under different conditions. The two devices have a similar gate length of about 50 nm. The device recessed at high bias (140 V in Fig. 6b, reported in [4]) shows slight trenching when compared with the flat channel observed in Fig. 6a which is obtained at 120 V and reported in [5]. This indicates that trenching, as a consequence of dry etch, will carry on to the finished device and most likely affect the device characteristics.

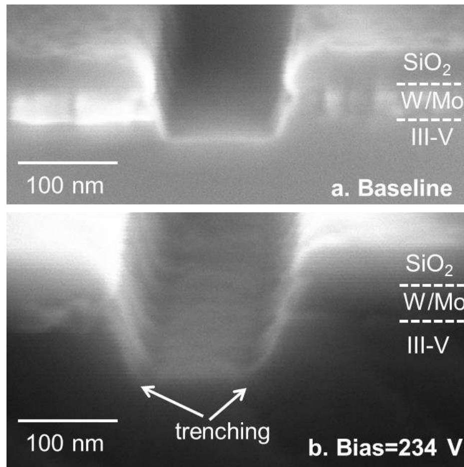

Fig. 5 Cross-section SEM images of dry etched samples using (a) baseline III-V etch conditions and (b) higher bias condition at 234 V. The recess opening is 100 nm.

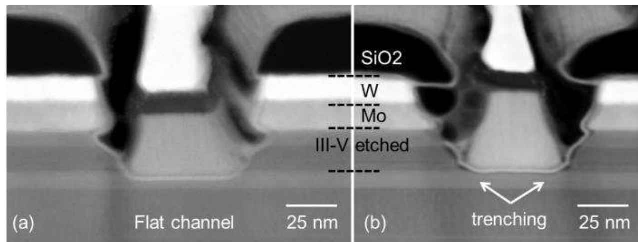

Fig. 6 TEM cross sectional images of finished self-aligned InGaAs MOSFETs. (a) etched under baseline conditions with a final 4 nm channel thickness. (b) etched at a higher substrate bias (140 V) and a final 8 nm channel thickness. Increased bias results in observable trenching at the two ends of the channel.

DIGITAL ETCH CALIBRATION

Cl_2-based RIE etches InGaAs, InAlAs and InP with comparable etch rate. Lack of selectivity is a problem for precision thickness control. To address this problem, our process features a novel 2-step III-V etching method. The concept is depicted in Fig. 7. For illustration purposes, it is adequate to simplify the III-V layer structure into a simple one consisting of a n^+-InGaAs cap on top of a thin InP etch stop layer placed right above an InGaAs channel.

In a first step, the III-V dry etch is stopped a few nm above the InP layer by time control. The final location need not be precise. From this point on, digital etch is used to remove material in a controlled manner at an etch rate of ~1 nm per cycle [7]. Multiple cycles of digital etch are performed (Fig. 7 a-c) until the desired final recess depth is obtained.

To know when to stop the digital etch, we rely on precisely locating the bottom InGaAs/InP interface right above the channel. For this, we adopt a calibration method that uses a highly selective wet etchant for InGaAs (and InAlAs) on InP [14]. The sequence is shown in the flowchart in Fig. 7. A test sample from the same heterostructure is patterned with photoresist and joined to the real device sample for III-V dry etching. The photoresist is then removed by acetone. This test sample, as shown in Fig. 7a, is used to determine the number of digital etch cycles "N" that is needed to reach the lower InP interface from the point left after dry etch.

After a certain number of digital etch cycles are performed (Fig. 7b), we cleave a small portion of the test sample and dip it in H_2O_2:H_3PO_4:H_2O (1:1:25) for 30 s. The solution etches InGaAs/InAlAs over InP with a selectivity of at least 100 to 1. This is followed by an inspection (Fig. 7c). If even a small amount of InP is left, this etchant only removes the InGaAs cap and the sample appears featureless under an optical microscope. On the other hand, if the InP barrier has been breached, the H_3PO_4 solution produces readily visible trenches in the underlying InGaAs layer. Using this technique in a methodic manner, one can determine the precise number of cycles "N" that it takes to just breach through the InP barrier. This locates the bottom InGaAs/InP interface with a precision equal to that of digital etch, about 1 nm. With this information, one can then estimate the number of cycles that it takes to achieve a given channel thickness, whether buried channel or surface channel, in the actual device sample.

We have verified this method by examining the cross section of finished devices through TEM in two different runs with different final channel thickness targets, as shown in Fig. 6. The respective TEM image confirms the targeted channel thickness (4 nm and 8 nm, respectively). The method depicted in Fig. 7 has the advantage of being fast (w.r.t. TEM) and accurate (w.r.t step profiling).

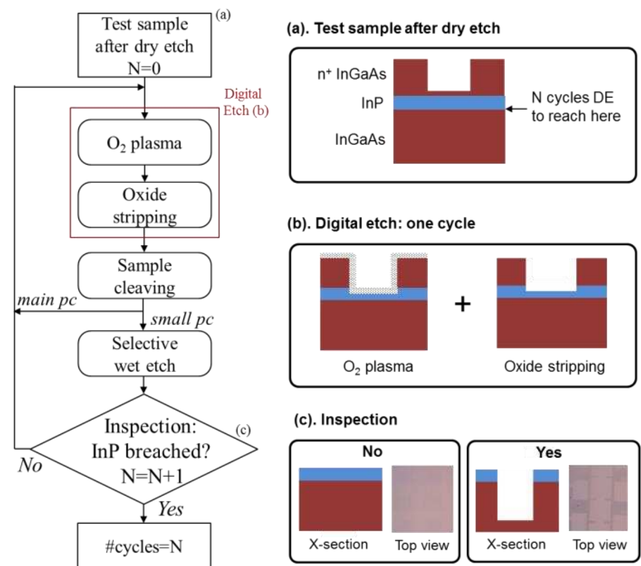

Fig. 7 Left: flowchart of digital etch calibration process on test sample. Right: schematic illustration for (a) calibration sample after dry etch, (b) one digital etch cycle, and (c) inspection using optical microscope.

W BARRIER FOR OHMIC CONTACTS

Our self-aligned InGaAs MOSFET process features a W/Mo bilayer ohmic contact. This approach was developed to correct the formation of a deep lateral undercut during F-based RIE in our first-generation devices that featured pure Mo contacts [3]. Fig. 8a shows a deep gash of a length of ~100 nm emerging from the edge of the contact. We have found that this originates on an interfacial Mo oxide layer of a thickness of about 10 nm that is formed during SiO_2 deposition. The etch rate of this interfacial layer during F-based RIE is much faster than Mo.

A solution to this problem was found by inserting a thin W cap layer above the Mo in the same sputtering step. W oxidizes

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much more slowly than Mo while featuring similar dry etching characteristics in F-based RIE [3]. As shown in Fig. 8b, F-based RIE does not cause any lateral undercut and yields nearly vertical ohmic contact sidewalls. This is critical for tight-pitch contact fabrication [4-5]. For the device with gate length of 20 nm, the contact-to-contact spacing is about 50 nm (Fig. 8b).

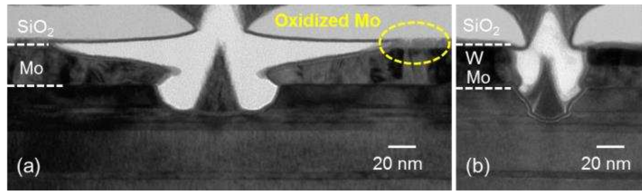

Fig. 8 Cross sectional TEM images of two MOSFETs: (a) with single layer of Mo contact [3], and (b) composite W/Mo contact [4-5].

DEVICE CHARACTERISTICS

The electrical characteristics of a typical device fabricated by this method are shown in Figs. 9-10. This device has gate length L_g=120 nm, and final channel thickness t_c=8 nm ($In_{0.7}Ga_{0.3}As/InAs/In_{0.7}Ga_{0.3}As$ with thickness of 1/2/5 nm). The III-V dry recess are at 140 V (Fig.6b and [4]). The subthreshold characteristics are shown in Fig. 9a. Minimum subthreshold swings for V_{ds}=0.05 and 0.5 V of 83 mV/dec and 95 mV/dec respectively, are obtained. These are excellent values for this device dimension. Drain-induced barrier lowering (DIBL) is 120 mV/V. The degradation of subthreshold swing and I_{off} at high V_{ds} that is observed is caused by BTBT and parasitic bipolar gain effect [16]. Despite the use of a very thin gate insulator (2.5 nm HfO_2, EOT~0.5 nm), very low gate leakage density for this device is observed. It is below 10^{-2} A/cm^2 for the gate voltage span as shown in Fig. 9b.

Output characteristics of a fabricated L_g=20 nm MOSFET with about 15 nm separation between the edge of the ohmic contacts and the edge of the gate (Fig. 8b) demonstrate the potential of our technology for highly scalable tight-pitch InGaAs MOSFET fabrication (Fig. 10). The R_{on} of this device is 224 Ω.μm.

Another device with L_g=80 nm and t_c=9 nm fabricated on the same heterostrcuture and recessed at 120 V for trenching immunity delivers very low R_{on} of 190 Ω.μm and a record transconductance of $g_{m,max}$= 3.1 mS/μm [5], as shown in Figs. 11 (a) and (b).

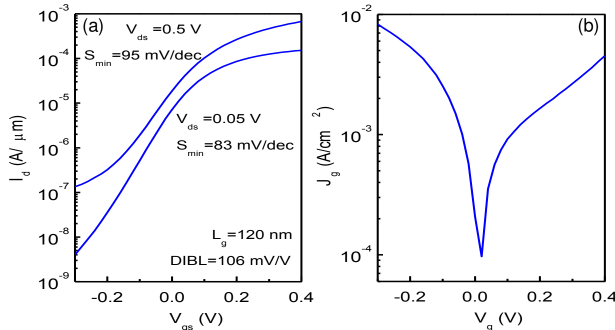

Fig. 9 (a) Transfer characteristics of InGaAs MOSFET with L_g=120 nm. (b) Gate leakage density of the InGaAs MOSFET [4].

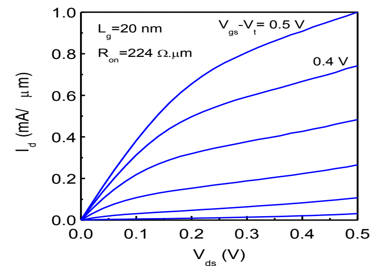

Fig. 10 Output characteristics of InGaAs MOSFET with L_g=20 nm [4].

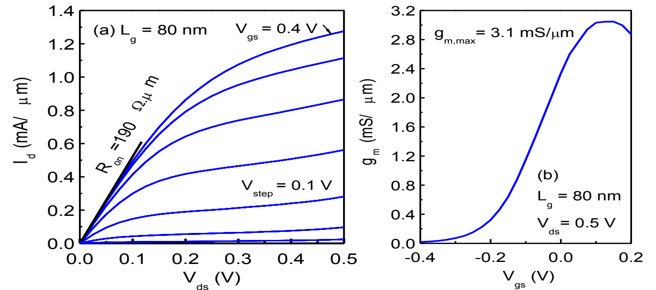

Fig. 11 (a) Transconductance and (b) output characteristics of InGaAs MOSFET with L_g=80 nm and channel thickness t_c= 9 nm [5].

CONCLUSIONS

This paper describes a novel dry-etched recessed-gate process to fabricate scaled self-aligned InGaAs MOSFETs. We achieve a smooth etched intrinsic surface with minimum trenching. Recess depth control within 1 nm accuracy can be achieved. Fabricated devices demonstrate excellent electrical characteristics and show case the potential of InGaAs for future logic MOSFET applications.

ACKNOWLEDGEMENT

This work is supported by Donner Chair at MIT, Defense Threat Reduction Agency Contract HDTRA1-14-1-0057, NSF Award 0939514 (E3S STC), and the MIT SMART/LEES program. Device fabrication was performed at MIT's Microsystems Technology Laboratories and SEBL.

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