Current Dispersion in Short Channel AlGaN/GaN HEMTs.

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Abstract

This work presents investigations of the dynamic behavior of short channel AlGaN/GaN HEMTs with Lg varying from 100 nm to 200 nm. Transistors were fabricated using AlGaN/GaN epitaxial structures with nominally the same GaN:Fe buffer layer and AlGaN barrier layers with different thicknesses and Al mole fractions. DC measurements of fabricated transistors showed similar performance for all epitaxial structures as well as for all L_g. Dynamic I-V analysis (DIVA) revealed significant differences between transistors with different L_g fabricated on the same epitaxial structure, as well as between transistors with the same L_g fabricated on different epitaxial structures. Differences in the amount of drain current reduction, $g_{m_{max}}$ degradation and knee voltage walkout at gate lag conditions were observed. The differences are attributed to the traps located in the area under the gate electrode. The physical mechanism of the observed phenomena was related to the interaction of several effects that influence electron mobility in the channel.

INTRODUCTION

During the last decade output power, efficiency, operation frequency and reliability of GaN HEMTs increased significantly. Today this technology is a good candidate for advanced high frequency space applications, such as Ka-band broadband satellite communication systems. The advantages of using GaN HEMTs instead of conventional TWTAs in the transmitting part of the system are smaller dimensions, lower energy consumption and the possibility of creating active antenna arrays. In the receiving part of the system, the replacement of GaAs pHEMT MMICs by GaN LNAs facilitates less complex and more robust LNAs as protecting diodes at the input can be omitted. Despite of the relatively high maturity of GaN technology, the development of optimized Ka-band PA and LNA MMICs requires the simultaneous handling of contradictory technical demands. For example, the gate-to-channel distance has to be decreased for short gate transistors to avoid short channel effects. However, this usually leads to a reduced electron concentration in the channel. An increase of Al-concentration in the barrier may compensate this effect; on the other hand, increasing the Al concentration beyond a certain threshold compromises crystalline quality of the AlGaN layer and subsequently leads to gate lag phenomena which cause a decreasing RF output power and a reduction of transistor reliability and lifetime [1]. In order to find the optimal combination of L_g and epitaxial structure for the Ka-band frequency range, transistors with different L_g were fabricated on the epitaxial structures with different configurations of barrier layers.

EXPERIMENT

Epitaxial structures were grown by low-pressure MOVPE on semi-insulating 4H-SiC substrates. Table 1 describes the detailed design of the structures. All three structures have nominally the same GaN:Fe buffer layer, the thickness of the channel layer is designed so that the Fe concentration decaying from the buffer drops below the SIMS detection limit at the 2DEG position. Different configurations of AlGaN barrier layers with varying Al content and thickness were designed in order to keep the sheet resistance in the range Rs ~ 350 – 400 Ohm/□. An n-type GaN cap layer was introduced to prevent potential surface instabilities. After ohmic contact formation all wafers were passivated with 100 nm thick SiN_x deposited at 325 °C by PECVD. Details of gate processing can be found elsewhere [2]. E-beam exposure with the same dose, but different layout dimensions was used in order to obtain gate trenches with different widths. As it is hard to pinch-off the transistors fabricated on epitaxial structures with thick AlGaN layer (structures B and C) with short gates, only gates with length 150 nm and 200 nm were fabricated on

13

TABLE I
EPITAXIAL STRUCTURES USED IN EXPERIMENT

Name	Cap	Barrier	Channel	Buffer	R_s (Ohm/□)
A	2 nm GaN	uid 10 nm $Al_{0.32}GaN$	820 nm GaN	~900 nm GaN:Fe	350
B	2 nm GaN	uid 15 nm $Al_{0.28}GaN$	820 nm GaN	~1200 nm GaN:Fe	360
C	5 nm GaN	uid 18 nm $Al_{0.24}GaN$	820 nm GaN	~1200 nm GaN:Fe	420

TABLE II
DESIGN OF EXPERIMENT

Epitaxial structure	L_g (nm)			
	100	130	150	200
A	x	x	x	x
B			x	x
C			x	x

those wafers. The full experimental plan is shown in Table 2. After wafer processing DC, load-pull and DIVA measurements were performed in order to estimate the electrical performance of the fabricated transistors.

GATE LAG EVALUATION METHOD

For the evaluation of gate lag phenomena DIVA measurements were performed at two quiescent bias points. The first point at V_{ds} = 0 V and V_{gs} = 0 V (0,0) was used for evaluation of reference drain current. The second point at V_{ds} = 0 V and V_{gs} = -7 V (0,-7) was used for measurement of drain current at gate lag conditions. The drain current was measured during the application of synchronized gate and drain voltage pulses with 200 ns length. The conventional way of gate lag estimation is to divide the drain current at V_{ds} = 0 V, $V_{gs} = V_{th} - 2$ V quiescent bias point (gate lag conditions) by the drain current obtained after pulsing from the V_{ds} = 0 V, V_{gs} = 0 V quiescent bias point to certain positions within the output characteristics (i.e. at bias points of different large-signal operation modes, for example at $V_{ds} = V_k$ (knee voltage) etc.). As the operation point of a transistor depends on pinch-off voltage, this method is sensitive to possible pinch-off voltage shifts of the specific transistor. Extraction of drain current at fixed voltages V_{gs} for transistors with different L_g will not provide a fair comparison of performance due to different pinch-off voltages at (0,0) quiescent bias conditions (Fig. 1 top). In order to overcome this issue, DIVA output characteristics were measured with a quite high resolution (V_{gs} steps of 0.1 V). From these measurements the transfer characteristics at a given drain bias can be easily reconstructed. Consequently the gate-lag was evaluated along the whole transfer curve at V_{ds} = 10 V (Fig. 1 bottom). Another advantage of high resolution DIVA evaluation is the possibility to evaluate transconductance curves and estimate maximum transconductance (gm_{max}) (Fig. 2).

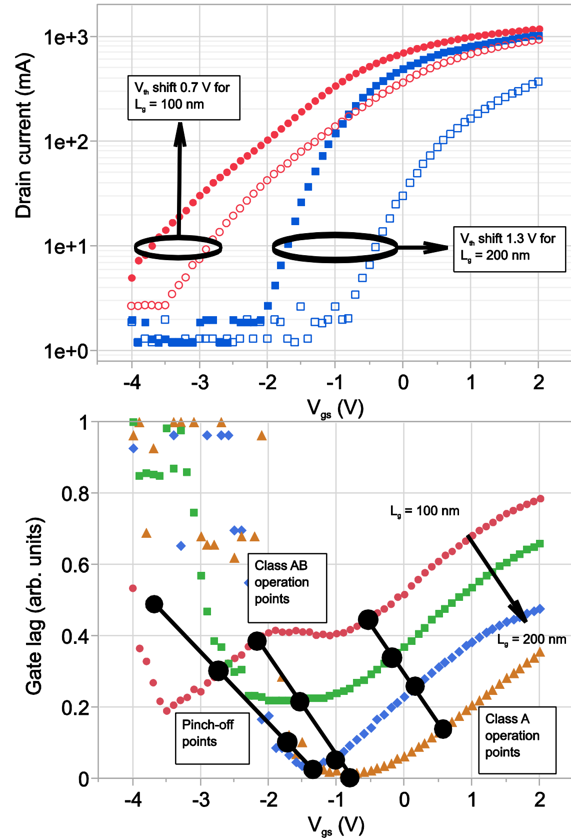

Figure 1 – Transfer characteristics derived at V_{ds} = 10 V (top) for transistors on epitaxial structure A evaluated at (0, 0) quiescent bias conditions (filled symbols) and (0, -7) bias conditions (empty symbols) for transistors with L_g = 100 nm (red) and 200 nm (blue). Gate lag (bottom) for transistors with L_g = 100 nm (red), 130 nm (green), 150 nm (blue) and 200 nm (orange) fabricated on epitaxial structure A.

DEPENDENCE OF GATE LAG ON L_G AND EPITAXIAL STRUCTURE

As can be seen from Figs. 1, 2 and 3 significant differences in the amount of gate lag, knee walkout and gm_{max} degradation were observed under the gate lag conditions between transistors with different L_g fabricated on epitaxial structure A. Transistors with shorter gates demonstrate less gate lag, less knee walkout and lower gm_{max} degradation under gate lag conditions as compared to longer gate devices. Later the similar tendency was observed for structures B and C as well. Also, it was observed that for transistors with the same L_g fabricated on different epitaxial structures knee walkout decreases from structure A to structure C (Fig. 4). In order to explain the phenomena observed at the gate lag conditions, electron mobility degradation in the region under the gate is proposed.

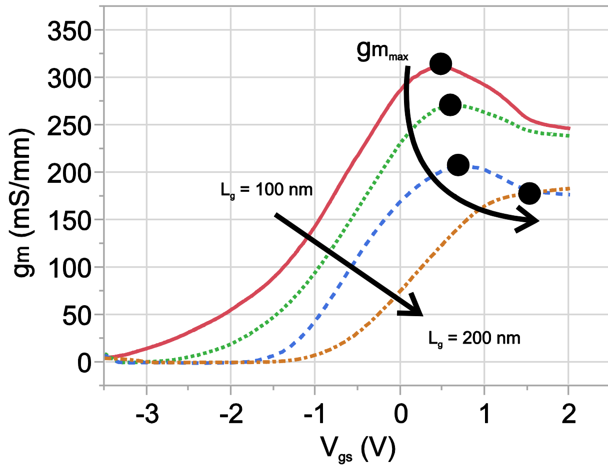

Figure 2 – Transconductance at V_{ds} = 10 V of transistors on epitaxial structure A measured at (0, -7) bias conditions, L_g = 100 nm (solid line), 130 nm (dotted line), 150 nm (dashed line) and 200 nm (dot-dashed line)

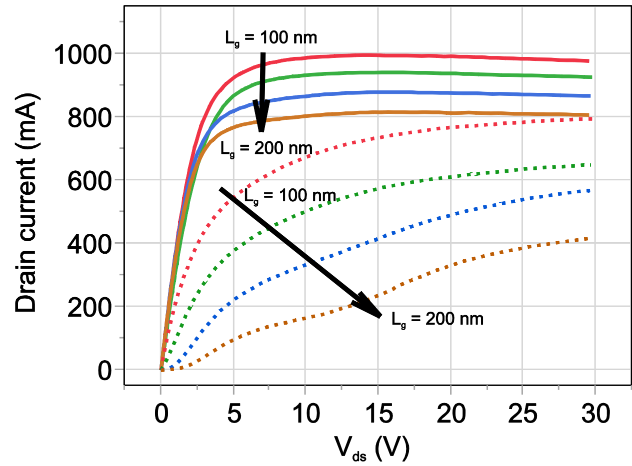

Figure 3 – Knee walkout dependence on the L_g for transistors on epitaxial structure A for (0, 0) quiescent bias conditions (solid lines) and (0, -7) quiescent bias conditions (dotted lines), L_g = 100 nm (red), 130 nm (green), 150 nm (blue) and 200 nm (orange).

Physical Mechanism of Gate Lag in Short Channel Transistors

As it was shown before [3], the presence of traps in the area under the gate electrode can cause pinch-off voltage shift and be the cause of gate lag in AlGaN/GaN HEMTs. A first sign of different influence of charged traps on transistors with different L_g can be observed in Fig. 1 (top). Transistors with 200 nm gate experience a pinch-off voltage shift by 1.3 V after pulsing them from a (0,-7) quiescent bias, whereas for the transistors with 100 nm gate the shift is reduced to 0.7 V. Evaluation of transfer and output characteristics at different quiescent bias conditions reveals, that transistors with different L_g fabricated on the same epitaxial structure show similar gm_{max} and V_k at (0,0) quiescent bias point. Whereas at gate lag conditions a significantly different shift of V_k and different degradation of gm_{max} can be observed (Figs. 2 and 3). As both of these parameters depend on electron mobility, the decrease of gm_{max} and shift of V_k to positive direction indicate a mobility reduction. The strong dependence of knee walkout, pinch-off shift and gm_{max} degradation on L_g leads to the conclusion that the area under the gate electrode is affected by the electron mobility reduction. As it was shown before [4, 5], the electron mobility under the gate area can be significantly decreased by presence of transverse electric field created by charged traps located in the vicinity of the 2DEG (which is the case for gate lag condition). Another observation that supports the proposed mechanism is that with decreasing Al content (and therefore increasing crystalline quality of semiconductor under the gate) knee walkout at the gate lag conditions decreases due to less traps in the material (Fig. 4). The observed dependence of V_k on the density of defect states is also provided in [5]. The explanation of the difference in electron mobility degradation in the transistors with different L_g is shown in Fig. 5. Electrons may pass through the gated region by experiencing physically different conduction properties due to velocity overshoot, scattering of electrons in higher valleys or scattering on ionized impurities in case of traveling in the vicinity of buffer layer. Since velocity overshoot effects were reported for GaN HEMTs with L_g = 120 nm [6], we can propose the following mechanism of electron transport in short channel devices. For the short gate devices, the amount of electrons moving in the Γ valley is maximal (due to ballistic transport through the area with increased transverses electric field), as compared to devices with longer gates (where part of the electrons are heated up by transverse electric fields of charged traps and therefore pushed in higher valleys where they are moving with lower drift velocities). In order to confirm the above mentioned mechanism, physical simulation taking into account the dependence of electron temperature on electric field (i.e. hydrodynamic model)

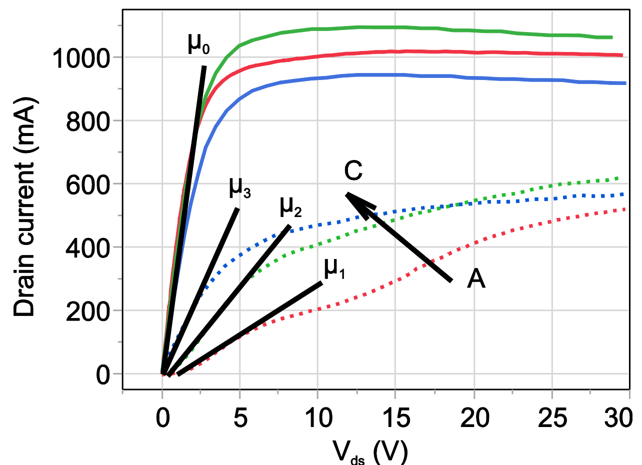

Figure 4 – Knee walkout dependence on the epitaxial structure for transistors with L_g = 200 nm at (0, 0) quiescent bias conditions (solid lines) and (0, -7) bias conditions (dotted lines), structure A (red), B (green) and C (blue).

13

should be performed. Another effect that can cause different reduction of electron mobility for devices with different L_g is scattering of electrons on impurities in the buffer layer. As the area with charged traps is proportional to L_g, transistors with longer gates will deplete the 2DEG by charged traps more efficiently (region limited by dashed line in Fig. 5). The amount of electrons pushed in the area close to the doped buffer (and therefore experiencing more scattering on the ionized impurities from the buffer layer) will be higher, as compared to short channel devices. In order to confirm this effect, physical simulation using the conventional drift-diffusion model was carried out. During the simulation an influence of gate length on the knee walkout was found, but the simulated dependence of drain current reduction in transistors with different L_g was much weaker than that observed during the experiment. The latter finding suggests that the velocity overshoot mechanism discussed above might be dominant for the devices with L_g as used in current work.

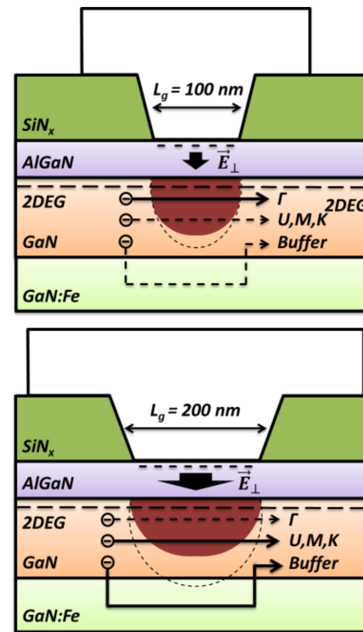

Figure 5 – Difference in electron paths under the gate area at (0,-7) quiescent bias conditions for transistors with different L_g (area affected by strong transverse electric field is highlighted by brown, region depleted by charged traps limited by dashed line).

CONCLUSIONS

The dynamic behavior of AlGaN/GaN HEMTs with different L_g, fabricated on the epitaxial structures with different AlGaN barrier layers was studied under gate lag conditions. A significant reduction of gate lag, knee walkout and gm_{max} degradation was observed on devices with small L_g regardless of the epitaxial structure used. The reduced sensitivity of short gate devices to gate lagging was ascribed to the smaller area affected by strong transverse electric fields created by charged traps under the gate electrode. The interdependence of velocity overshoot increasing longitudinal electron velocity in short channels with increased impurity scattering in the buffer layer was proposed as mechanism explaining the different degradation of electron mobility in devices with different L_g.

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REFERENCES

[1] E. Zanoni, M. Meneghini, A. Chini, D. Marcon and G. Meneghesso "AlGaN/GaN-based HEMTs failure physics and reliability: Mechanismsaffecting gate edge and Schottky junction", IEEE Trans. Electron Devices, vol. 60, pp.3119 -3131, 2013

[2] K. Y. Osipov, S. A. Chevtchenko, O. Bengtsson, P. Kurpas, F. Brunner, N. Kemf and J. Würfl, "Implementation of Slanted Sidewall Gates Technology in the Fabrication of S-, X-, and Ka-band AlGaN/GaN HEMTs", CS Mantech Conf., 2014.

[3] M. Meneghini, N. Ronchi, A. Stocco, G. Meneghesso, Umesh. K. Mishra, Yi Pei, and E. Zanoni "Investigation of Trapping and Hot-Electron Effects in GaN HEMTs by Means of a Combined Electrooptical Method", IEEE Trans. Electron Devices, vol. 58, pp.2996 -3003, 2011

[4] P. D. Ye, B. Yang, K. K. Ng, and J. Bude "GaN metal-oxide-semiconductor high-electron-mobility-transistor with atomic layer deposited Al2O3 as gate dielectric", Appl. Phys. Let., vol. 86, 063501 (2005)

[5] W. D. Hu, X. S. Chen, Z. J. Quan, X. M. Zhang, Y. Huang, C. S. Xia, and W. Lu "Simulation and optimization of GaN-based metal-oxide-semiconductor high-electron-mobility-transistor using field-dependent drift velocity model", J. Appl. Phys, vol. 102, 034502 (2007)

[6] M. Singh, Y. R. Wu and J. Singh "Velocity Overshoot Effects and Scaling Issues in III–V Nitrides", IEEE Trans. Electron Devices, vol. 52, pp.311 -316, 2005

ACRONYMS

RF: Radio Frequency
DC: Direct Current
HEMT: High Electron Mobility Transistor
2DEG: 2 Dimensional Electron Gas
MMIC: Monolithic Microwave Integrated Circuit
DIVA: Dynamic IV Analysis
TWTA: Traveling Wave Tube Amplifier
L_g: Gate Length
gm_{max}: Maximum Transconductance
V_k: Knee Voltage
V_{th}: Threshold Voltage
V_{ds}: Drain-Source Voltage
V_{gs}: Gate-Source Voltage