Field Plate Models Applied to Manufacturability and for RF Analysis

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Keywords: Field plate, electric field, small-signal model

Abstract

Electric field sensitivity analysis with respect to process controlled parameters and material controlled parameters of channel charge, field plate to channel distance, and transition angle between gate and field plate has been performed. Small-signal model topology for gate connected and source connected field plated devices has been generated based on a two transistor model for a transistor with a field plate.

INTRODUCTION

Field plates are now commonly used for electric field engineering in both high frequency and power transistors. With proper field plate design, significant performance improvements can be obtained [1]. Despite the wide spread adoption of field plates, only recently has a simplified field plate model that captures the majority of the physics been introduced [2,3].

It is the purpose of this work to demonstrate how the simplified field plate model in [2,3] can be used for an electric field sensitivity analysis on transition angle $(\pi\varphi)$ between field plate and gate, field plate to channel spacing a_1, and charge in the channel σ in the off-state (see Fig. 1). Then modifications to the two transistor model for a transistor with a field plate used in [2] for DC analysis are performed to produce a small-signal model topology for gate connected and source connected field plate configurations.

FIELD PLATE MODEL

The field plate model introduced in [2,3] will be developed from a charge imaging standpoint during the presentation. The model is only valid for long field plate designs. A natural definition of "long" comes from the model through the aspect ratio $l_{FP}/a_1 \geq 6$, where l_{FP} is the field plate length (including the slant portion). An aspect ratio ≥ 6 follows the well-known aspect ratio design rule used for gate length designs now being seen to also apply to field plates. It also supports the view of analyzing the field plate and gate as a combination of two transistors in series with one transistor representing the gate and the second transistor representing the field plate as shown in Figure 2.

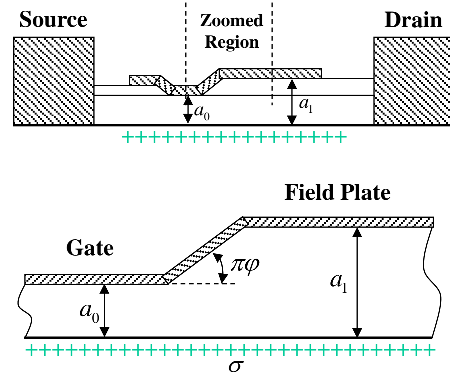

Figure 1. Definition of field plate model parameters.

The model also shows that independent of transition angle $\pi\varphi$, the pinch-off voltage of the field plate can be viewed as the maximum channel potential between the gate electrode and channel. Therefore, the difference between the potential applied to the field plate and the field plate pinch-off voltage can be view as the drain voltage applied to the transistor representing the gate electrode (Q1) in the two transistor model as shown in Fig. 2.

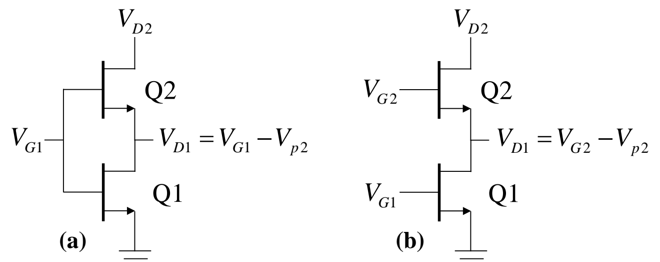

Figure 2. Two transistor model for a transistor with a field plate. (a) gate connected field plate. (b) Field plate not gate connected.

Building on these results, it will be shown how an electric field sensitivity analysis on process controlled parameters and material parameters can be performed. Although the two transistor model works well for DC analysis, it will be shown that modifications are needed for proper small-signal analysis due to the saturation velocity region extending under the entire field plate under certain bias conditions.

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ELECTRIC FIELD SENSITIVITY ANALYSIS

In order to produce a stable repeatable product, understanding design sensitivities to process controlled parameters and material controlled parameters is key. Using the field plate model for long field plate devices introduced in [3] the electric field $(\mathcal{E})$ in the device can be written as

$$\mathcal{E}[z] = (\sigma/\varepsilon) f[a_1/a_0, \varphi, z] \tag{1.1}$$

where ε is the permittivity of the system, a_0 is the gate to channel spacing, and z is the position in the device. All other parameters have been defined. Variation in $\mathcal{E}$ with changes in its dependent parameters can be expressed as

$$\Delta\mathcal{E} \approx \frac{\partial\mathcal{E}}{\partial(a_1/a_0)}\Delta(a_1/a_0) + \frac{\partial\mathcal{E}}{\partial\varphi}\Delta\varphi + \frac{\partial\mathcal{E}}{\partial(\sigma/\varepsilon)}\Delta(\sigma/\varepsilon) \tag{1.2}$$

Therefore, changes in electric field or the electric field sensitivity defined as $\Delta\mathcal{E}/\mathcal{E}$ can be determined once the derivatives of $\mathcal{E}$ with respect to the dependent parameters are obtained.

The dependence of $\mathcal{E}$ on channel charge is the easiest sensitivity to evaluate and is given as

$$\Delta\mathcal{E}/\mathcal{E} = \quad \sigma/\sigma \tag{1.3}$$

The electric field in all regions of the device is directly impacted by any change in channel charge and therefore tight limits on σ are required for tight control of $\mathcal{E}$.

Unfortunately, the electric field sensitivity on a_1/a_0 and $\pi\varphi$ requires evaluating the electric field integral given in [3]. The model was used to determine the electric field in the channel for different field plate to channel distances for two transition angles: 30° and 90°. Simulations of the electric field in the channel were also performed as a function of transition angle $\pi\varphi$ for $a_1/a_0 = 4$ and $a_1/a_0 = 8$.

The sensitivity of the magnitude of the peak electric field in the channel $\left(|\mathcal{E}|_p \equiv \mathcal{E}_p\right)$ to all three parameters for a 10% change in each parameters is shown in Fig. 3. There are several items to observe in Fig. 3. First, if each parameter has the same percent change, then $\mathcal{E}_p$ would be most sensitive to σ, followed by a_1/a_0 and finally $\pi\varphi$. Second, $\mathcal{E}_p$ sensitivity on transition angle increases with increased field plate to channel spacing. $\mathcal{E}_p$ is also more sensitive to transition angle changes below 45° compare to angles above 45°.

The electric field sensitivity in other parts of the device can be investigated using the same approach. Same trends for electric field sensitivity are expected although the magnitudes may differ.

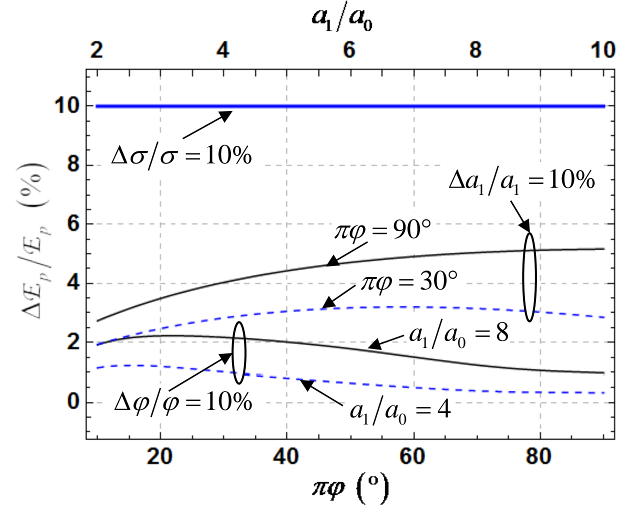

Figure 3. Electric field sensitivity for a 10% change in channel charge (σ), normalized field plate to channel spacing (a_1/a_0), and transition angle $(\pi\varphi)$.

SMALL-SIGNAL MODEL TOPOLOGY

The two transistor model used in [2] for DC analysis and shown in Fig. 2 will now be modified for small-signal AC analysis. If two small-signal models are combined without considering semiconductor device physics, the model shown in Fig. 4 results. For this model to become useful, the field plate connection (gate or source represented by X in the diagram) and the bias condition need to specified.

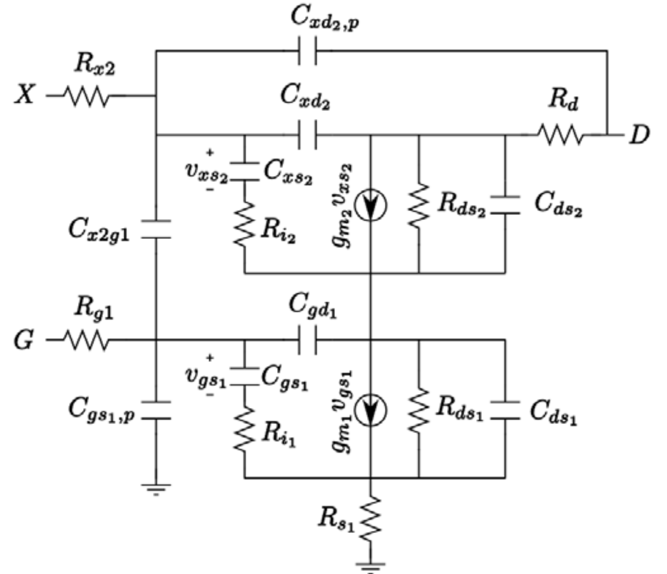

Figure 4. Initial two transistor small-signal model for a transistor with a field plate. Field plate connection (X) and bias condition still need to be specified.

For high voltage amplifiers, a reduced conduction angle is typically used to reduce dissipated power at the bias point

and for increased peak power added efficiency (PAE) under large signal drive. Therefore, the small-signal model will be developed around a deep Class AB bias condition.

In deep Class AB bias, the drain current is very small and the x-component of the electric field ($\mathcal{E}_x$) can be approximated by $\mathcal{E}_x$ in the off-state. Depending on the potential difference between the drain and field plate (V_{DFP}), two very different $\mathcal{E}_x$ profiles exist in the channel and are shown in Fig. 5. When V_{DFP} is less than the pinch-off voltage of the field plate ($|V_{P,FP}|$), a single peak in $\mathcal{E}_x$ is observed. This condition is very similar to a device without a field plate with the net positive fixed charge in the channel imaging on the gate only. The transistor representing the field plate is operating in the gradual channel regime ($\mathcal{E}_x \ll \mathcal{E}_y$) and the small-signal model is fairly straight forward to develop. When $V_{DFP} > |V_{P,FP}|$, two peaks are observed in $\mathcal{E}_x$. This condition does not exist in transistors without field plates. Due to paper length constraints, the small-signal model will only be developed for $V_{DFP} > |V_{P,FP}|$.

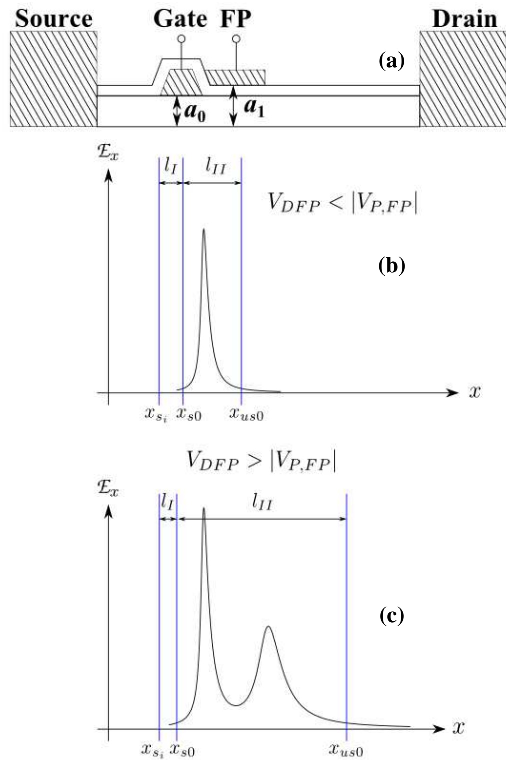

Figure 5. (a) Cross-section of a transistor with a field plate. Field plate connection left unspecified. (b) $\mathcal{E}_x$ profile in the channel for $V_{DFP} < |V_{P,FP}|$ and (c) $\mathcal{E}_x$ profile in the channel for $V_{DFP} > |V_{P,FP}|$.

$V_{DFP} > |V_{P,FP}|$ Operation

When $\mathcal{E}_x$ is above a critical field ($\mathcal{E}_x > \mathcal{E}_{crit} \approx v_{sat}/\mu$), carriers will travel at their saturation velocity (v_{sat}) instead of velocity equal to mobility (μ) times $\mathcal{E}_x$. In transistors without a field plate, the channel region that is in the saturated velocity regime (labeled l_{II} in Fig. 5) occupies a portion under the gate on the drain side and extends past the gate into the ungated access region. For a transistor with a field plated operated with $V_{DFP} > |V_{P,FP}|$, the saturated velocity of the channel starts near the drain edge of the gate and extends past the end of the field plate as shown in Fig. 5(c). Therefore, the transistor representing the gate can be viewed as a transistor without a field plate, but with a much larger than normal velocity saturated region. The transistor representing the field plate can no longer represents a discrete transistor with equivalent circuit parameters that can be measured. This has several consequences for the two transistor AC model:

1. R_{i2} represents the portion of the channel under the field plate not in velocity saturation and therefore does not exist.
2. Transport in the velocity saturation region under the field plate to x_{us0} is represented by an additional capacitance added to C_{gs1}, a phase term in transconductance g_{m1} and a magnitude factor for g_{m1} that is typically done for carrier transport in velocity saturated regions of transistors without field plate [4], thus eliminating C_{xs2} and g_{m2}.
3. C_{gd1} is significantly reduced since the modulation of charge at x_{ux0} by the gate that $C_{gd,I}$ represents is very small due to the large value of l_{II}. It will now be labeled C'_{gd1}
4. Similarly, $C_{ds,I}$ is very small due to the large value of l_{II} reducing the ability of drain voltage to modulate the non-velocity saturated region of the channel on the source side. An upper bound on the total C'_{ds} of field plate and gate is $\left(C_{ds1}^{-1} + C_{ds2}^{-1}\right)^{-1}$
5. Assuming the dominant cause of R_{ds1} is current through the buffer, R_{ds1} is significantly increased due to the large value of l_{II}. A lower bound on the total R'_{ds} of field plate and gate is $R_{ds1} + R_{ds2}$

To finalize the small-signal model, the connection of the field plate terminal needs to specified. First we will consider gate terminated field plates. Connecting terminal X in Fig. 4 to the gate results in the small-signal model for a gate terminated field plate shown in Fig. 6(a). The field plate to

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gate capacitance C_{x2g1} is shorted out due to this connection and the gate resistance becomes R_{g1} in parallel with R_{x2}. The more significant consequence of connecting the field plate to the gate is C_{xd2} and $C_{xd2,p}$ now become gate drain capacitances. In other words, despite a significant reduction in C_{gd1} due to large l_{II}, connecting the field plate to the gate negates this improvement.

The small-signal model for a source terminated field plate is shown in Fig. 6(b). Now C_{xd2} and $C_{xd2,p}$ become source drain capacitances and the small C_{gd1} due to large l_{II} is maintained. The price paid for this connection is the field plate to gate capacitance C_{x2g1} and no reduction in gate resistance. As shown in [5], reducing the overall C_{gd} is much more important for producing high gain at microwave frequencies than the added field plate to gate capacitance C_{x2g1}.

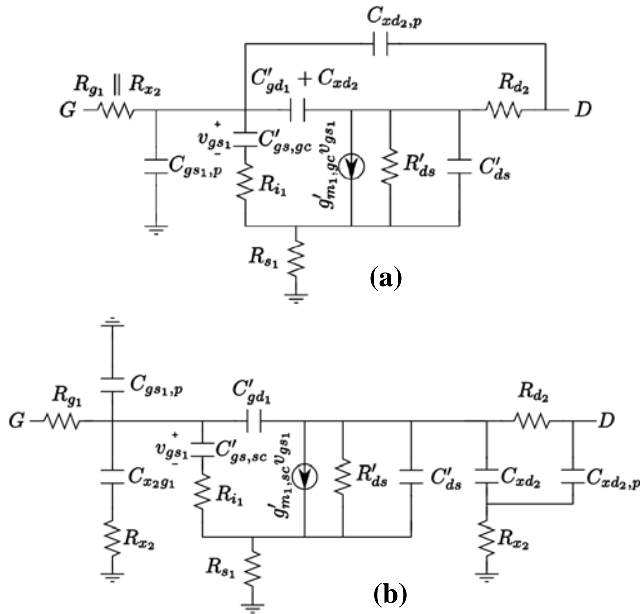

Figure 6. Small-signal model topology for (a) gate-connected field plate and (b) source connected field plate.

In both small-signal models, the primed parameters are different from their discrete transistor values. The unprimed parameters are the same or very close to the discrete transistor values. The parasitic field plate to drain and gate to source pad capacitances are accounted for through $C_{xd2,p}$ and $C_{gs1,p}$, respectively. Note the gate source capacitance and transconductance for the two models have been labeled differently. Their magnitudes are expected to be similar, but not the same. The difference comes mainly from the displacement current due to gate modulation of charge in the saturated velocity region. Extended analysis of this point is planned for publication elsewhere.

Although a specific design would need to be considered to make quantitative statements, general statements can be made between a gate connected field plate (GCFP) vs. a source connected field plate (SCFP). Due to the magnitudes of g_m and C_{gs} being similar between the two models and the reduction in C_{gd} for the SCFP model being offset by C_{x2g1} for the total input capacitance, a significant difference in the unity short circuit current gain frequency (f_τ) is not expected between the two configurations. Significant improvements are expected and have been shown [5] in power gain by the significant reduction in C_{gd} for the SCFP configuration compared to the GCFP configuration. The reduction in C_{gd} is even more important in high voltage gain devices where the Miller effect is significant.

CONCLUSIONS

The procedure for performing an electric field sensitivity analysis using the field plate models in [2,3] was demonstrated. If the channel charge, field plate to channel spacing and transition angle between gate and field plate are allowed to vary by the same percentage, then the electric field is most sensitive to channel charge. The deep class AB small-signal model topology for gate connected field plates and source connected field plates operating with a drain to field plate potential exceeding the field plate pinch-off voltage was developed. The reduction of C_{gd} total for source-connected field plate configurations is extremely important for high power gain, especially when high voltage gain devices are used.

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