

ESD Protection Device for HEMT MMICs

Jung-Tao Chung, Shinichiro Takatani, Cheng-Kuo Lin, Hsi-Tsung Lin, Shao-Chang Cheng, Shu-Hsiao Tsai, Cheng-Guan Yuan, Joseph S.M. Liu and Yu-Chi Wang

WIN Semiconductors Corp. Kuei Shan Hsiang, Tao Yuan Shien, 333, Taiwan, R.O.C

E-mail: jtchung@winfoundry.com, takatani@winfoundry.com

Phone: +886-3-3975999#1519

Keywords: high-electron mobility transistor (HEMT), electrostatic discharge (ESD), human body model (HBM)

Abstract

This study provides the way to realize high electron mobility transistors (HEMT) circuits with high level ESD protection with minimal impact on the chip size and cost. For ports operated under high voltage, the new multi-gate enhancement-mode HEMT power clamp device provides over 2kV human body mode (HBM) ESD protection in HEMT MMICs with large and designable turn-on voltages in the both direction. For ports operated under lower voltage, the series of modified P-N diode also provides over 2kV HBM ESD protection level with the 484 μm^2 device size.

I. INTRODUCTION

III-V high electron mobility transistors (HEMTs) have been widely used in Monolithic Microwave Integrated Circuits (MMICs) for power amplifiers (PA), low noise amplifiers (LNA), and switches. More recently, Silicon on insulators (SOIs) and RF CMOS transistor have been used for the MMIC applications including those used in cellular PA modules. In comparison with the Si-based technologies, the lack of suitable electrostatic discharge (ESD) protection devices with a small footprint is one of the major drawbacks for HEMT MMICs.

Conventionally, ESD protection circuits for HEMT MMICs are made of series-connected Schottky diodes. One way to shrink the footprint is to introduce the power clamp structure composed by enhancement mode HEMT with the gate connected to source with the resistor [1][2]. Furthermore, multi-gate layout enables even smaller device footprint compared with the conventional power clamp scheme in which single gate devices are connected in series [3][4]. The multi-gate power clamp has also been demonstrated that it can be used to protect RF switch circuit [5]. The other way to shrink the footprint is to replace the Schottky diodes by P-N junction diodes which have better current-conducting capability and higher trigger voltage.

In this study, the ESD protection capability of both multi-gate enhancement mode HEMT power clamp and the

optimized P-N junction diode are demonstrated. The layout is also illustrated to show the impact of the chip size is minimal.

II. MULTI-GATE POWER CLAMP

Fig.1 illustrates the dual-gate field effect transistor (FET) layout. The gate is connected to the source/drain with a resistor. The equivalent function block is illustrated in the Fig. 1(c). Since it can act as series connected diodes in the opposite direction, a large turn-on voltage of around 10 V is achieved in the both directions.

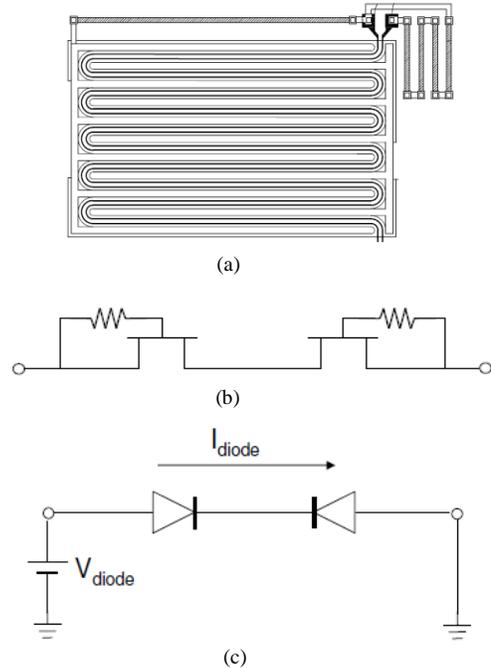


Fig.1. The (a) layout, (b) schematic, (c) equivalent function block of the dual-gate HEMT power clamp

A. TRANSMISSION LINE PULSE MEASUREMENT

The transmission line pulse (TLP) measurement is widely used to characterize the device voltage and current during

the ESD event. The TLP measurement result for the dual-gate HEMT power clamp is shown in Fig. 2. It is found that the TLP characteristics are sensitive to the gate recess etching condition. Fig. 2 shows the TLP characteristics for three different etching conditions. For the modified gate process (shown by the dash line in Fig. 2), TLP shows the triggering voltage (V_t) of around 17.5 V with the holding voltage (V_h) of 11V.

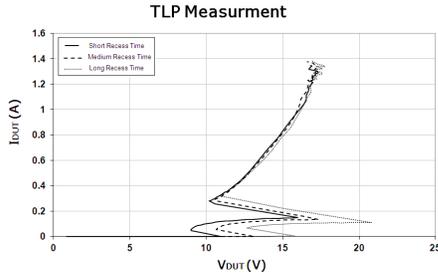


Fig.2. TLP measuring results

B. GATE MULTIPLICITY

The gate multiplicity and the connection of gate resistors are chosen for each electrical terminal to be protected depending on the polarity and magnitude of the DC/RF voltages applied to the terminal during operation. Fig.3 shows two types of multi-gate FET layout with different gate resistor connections and the same total gate width. The current turn-on characteristics are shown in Fig. 4. As expected the turn-on voltage increases as the number of gate multiplicity in the same polarity increases.

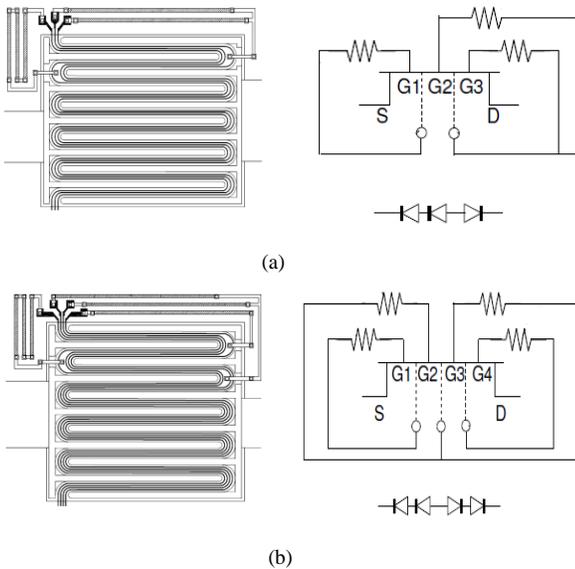


Fig.3. Examples of multi-gate clamp (a) Triple gate HEMT power clamp, (b) Quadruple gate HEMT power clamp

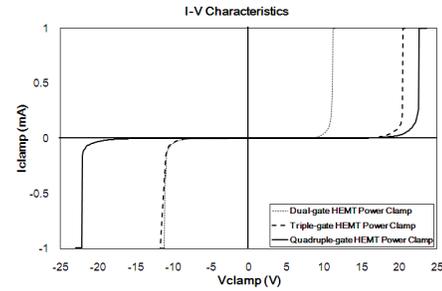


Fig. 4 I-V Characteristics of (a)Triple (b)Quadruple gate HEMT power clamp

Human Body Model (HBM) is the major product specification and commonly used for ESD protection capability evaluation. The HBM ESD protection capability of the above devices is evaluated and the results are summarized in Table. I. The HBM level can maintain the same for devices with different gate multiplicity.

TABLE I
HBM ESD PROTECTION LEVEL VERSUS DEVICE GATE PERIPHERY

Gate Periphery (um)	Dual-gate	Triple-gate	Quadruple-gate
HBM ESD Level (kV) (DUT : Multi-gate HEMT Clamp)	2.1	2	2

C. VERIFICATION

Capacitor is one of the weak points for HEMT MMICs. The ESD protection capability of the dual-gate power clamp with different total gate periphery is tested for two cases. One is for the power clamp device alone, and the other is the power clamp device connected to a 0.02-pF metal-insulator-metal (MIM) capacitor for protection. The schematic of the second case is attached in Fig. 5, and the result is shown in Table. II. HBM protection over 2kV is achieved for devices with the gate periphery 1000um or larger multi-gate power clamps. For the case with the MIM capacitor, the power clamp device was damaged prior to the capacitor. It proves that the MIM capacitor is well protected by the power clamp device.

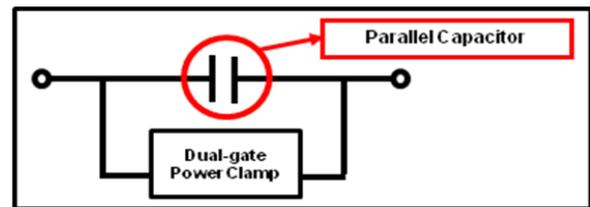


Fig. 5 Schematic of the capacitor which is parallel-connected to the dual-gate power clamp

TABLE II
HBM ESD PROTECTION LEVEL VERSUS DEVICE GATE PERIPHERY

Gate Periphery (um)	750	1000	1250	1500
HBM ESD Level (kV) (DUT : Dual-gate HEMT Clamp)	1.6	2.1	2.5	3.0
HBM ESD Level (kV) (DUT : Capacitor protected by dual-gate HEMT Clamp)	1.6	2.1	2.5	3.0

III. MODIFIED P-N JUNCTION DIODE

In addition to the multi-gate power clamp, the other approach is to utilize the modified P-N junction diode for ESD protection. Based on WIN semiconductors' BiHEMT technology which could integrate HBT and HEMT process in the same epi wafer, the modified P-N junction diode can be introduced to the top of the HEMT. The HBM ESD protection level versus ESD protection device size is shown in Fig. 6. Over 2kV HBM ESD protection level is achieved with the 484um² device size.

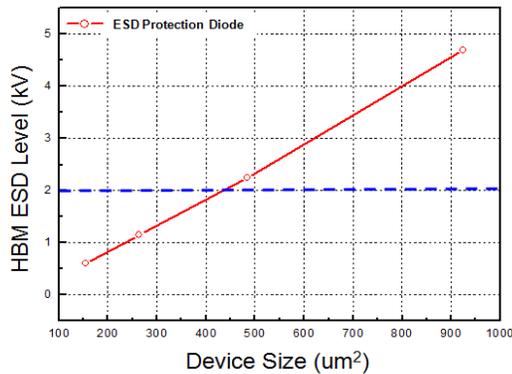


Fig.6 HBM ESD protection level versus ESD protection P-N diode size

In comparison with the multi-gate enhancement-mode HEMT power clamp, the device size is smaller but the turn-on voltage is only 1.2V. However, a series of diodes can be used to increase the turn on voltage. Fig7. shows the turn-on voltage of single diode and 8 diodes in series are 1.2V and 9.6V, respectively. Suitable number of diodes in series can be chosen to meet the requirement of DC supply voltage or voltage swing under RF operation.

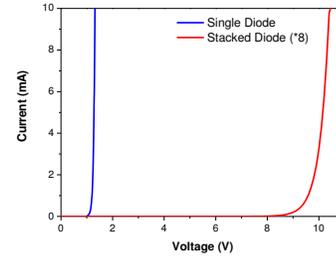


Fig. 7 B-C diode turn-on voltage comparison between single diode and a series of diodes

IV. CONCLUSION

In conclusion, the new multi-gate enhancement-mode HEMT power clamp device provides over 2kV HBM ESD protection in HEMT MMICs with large and designable turn-on voltages in the both direction. The P-N junction diode can also provide the same HBM ESD level with smaller size and lower turn-on voltage. Choosing BiHEMT technology, circuit designers can select the suitable ESD protection device for different ports depend on the operating voltage. Combination of both approaches is expected to realize GaAs MMICs with high level ESD protection with minimal impact on the chip size and cost.

ACKNOWLEDGEMENTS

The authors would like to thank the people that supported the device layout, wafer fabrication and measurement of WIN's layout, manufacturing teams, respectively.

REFERENCES

- [1] C.K. Lin, et al., "On-chip ESD Protection Circuit Using Enhancement-mode HEMT/MESFET Technology." U.S. Patent 7,679,870, issued March 16, 2010.
- [2] Q. Cui, et al., "Development of a New pHEMT-Based Electrostatic Discharge Protection Structure", IEEE TRANSACTIONS ON ELECTRON DEVICES, VOL.58, NO. 9, September 2011.
- [3] S. Takatani, et al., "Compound Semiconductor ESD Protection Devices." U.S. Patent 8,964,342, issued February 24, 2015.
- [4] S. Muthukrishnan, et al., "A Novel Clamp Based ESD Protection Structure for High Power RF Ports in GaAs pHEMT Process.", Compound Semiconductor Integrated Circuit Symposium (CSICS), 2011.
- [5] S. Takatani, et al., "Integrated Circuits with ESD Protection Devices." U.S. Patent 2014/0,231,875, published August 21, 2014.

ACRONYMS

HEMT: High Electron Mobility Transistors
ESD: Electro Static Discharge
HBM: Human Body Mode

