pHEMT Device Characterization for Current Transient Time Constant and Link to Error Vector Magnitude

S. Nedeljkovic, S. Hurtt, P. Hamilton, P. Litzenberg
Qorvo, 2300 NE Brookwood Parkway, Hillsboro, Oregon 97124
Phone: 503-615-9871 Email: Sonja.Nedeljkovic@qorvo.com

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Abstract

The most challenging design and materials issue for future wireless LAN circuits remains dynamic error vector magnitude, or DEVM. While circuit designers have some ability to overcome materials-based current transients, eventually manipulating the fundamental materials is necessary to meet increasingly demanding customer specifications for DEVM. Test methods we used to understand transient behavior of pHEMT device represent the link to circuit level performance while at the same time are used for evaluation of epi designs and epi vendors.

INTRODUCTION

In some of our early WLAN designs the challenges and rewards of DEVM control became obvious, manifesting in yield fluctuations. Extensive testing of different epi and device processes and designs made it clear that circuit performance was linked to both the epi and fab. However, the mechanism for epi and fab impacts on circuit performance was not clear. In this work, we will describe a single-FET characterization technique that predicts circuit-level challenges for DEVM control.

PURPOSE

This paper describes a measurement flow for single device characterization under DEVM conditions on high-volume production 0.5um ED mode pHEMT process with an AlGaAs Schottky layer. The technique used pulsed IV in a conceptually simple measurement that was fully descriptive of the problem, and the difference between devices. The measurement consists of three separate transient measurements. Each measurement is necessary to understand the contributions from each region of the device to total transient time constant. Understanding the source of the transient and trapping behavior and the correlation to DEVM performance helps design teams to make the connection to DEVM data on circuit level. The technique is also beneficial in epi design and supplier qualification. With device level characterization, it is possible to synthesize device and epi understanding to improve circuit performance and yield.

DEVM MEASUREMENT ON DEVICE LEVEL

DEVM was measured at final test and is correlated to a deviation of drain current from an expected value during the data burst. Delays in current response can be caused by charge-trapping process. Delays can further be added by circuit design when the design is optimized for a specific fab lot or epi supplier, but drift in the epi growth or fab process occurs. Thus, it was necessary to separate the influence of design and device performance on DEVM by defining an approach for device level characterization. We developed the capability for a conceptually simple measurement that was fully descriptive of the problem, and the difference between suppliers. The chronogram for DEVM test on device level is shown in Figure 1. The measurement is performed using Pulsed IV system (AMCAD) [1] where the transient response is obtained in real time.

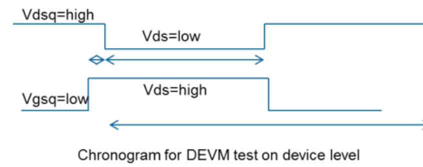

Figure 1: Chronogram for device level DEVM test

Transient response was measured on the device level under DEVM conditions for two different epi designs within a single fab process lot. The resulting Ids change over time shows clear differences in the drain current change versus time for materials A and B (Figure 2). This result matched what was observed on the circuit level, but measured delays in drain current response were still a combination of thermal, drain and gate lag time constants. The goal was to apply test conditions to separate factors contributing to the overall time constant. This would allow identification of the dominant cause of variation that contributes to performance variation in the finished circuit. The three-step test flow is shown in Figure 3.

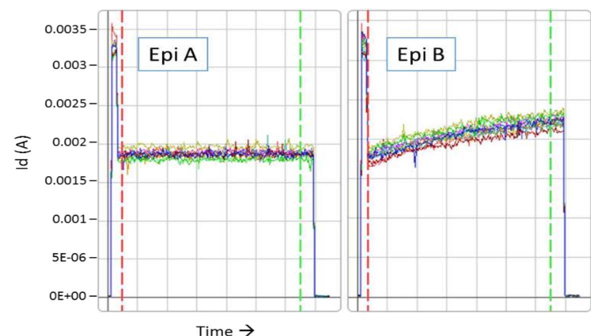

Figure 2: Transient response of device from two epi wafers under DEVM conditions

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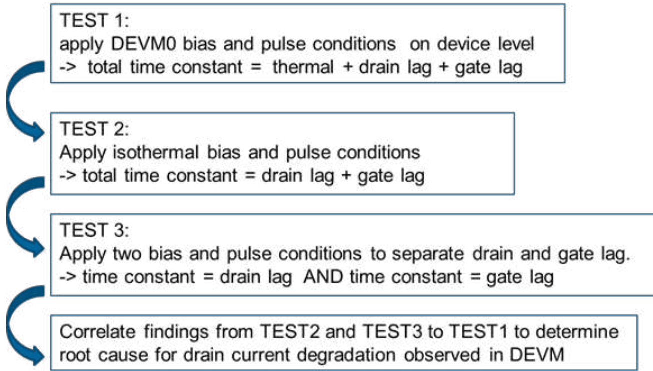

Figure 3: Test flow for transient characterization

In the test flow, each individual test isolates a region of the device to identify performance-limiting aspects of the fab and epi processes. Transient response on device level under DEVM conditions for two different epi vendors is shown on Figure 2 and it points to clear difference in drain current change versus time. This result matched what was observed on circuit level. To further understand the difference in device performance, test 2 was used to measure transient response under isothermal conditions [2]. This approach isolates trap behavior from thermal effects by pulsing under equal power dissipation. Principle for isothermal pulsed measurement for two power dissipation levels and chronogram for bias conditions are shown on Figure 4.

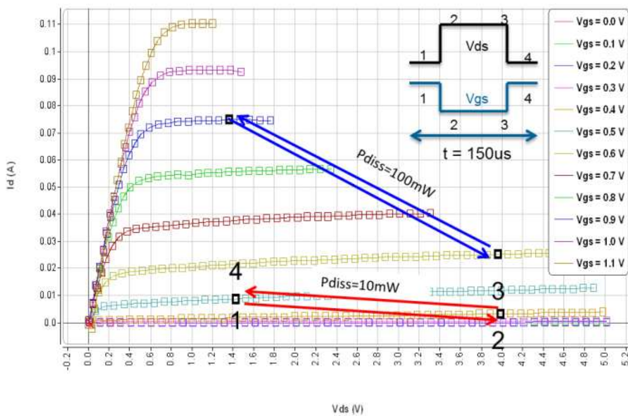

Figure 4: Quiescent point definition for isothermal measurements

The results of this test are shown in Figure 5 for two different power levels (Pdiss=0.033mW/um^2, 3.3mW/um^2) for two different epi types. The main difference between epi types is in the emission time constant, or de-trapping, while capture (trapping) time constatants are comparable.

In test 3, we applied conditions typical for gate and drain lag measurements [2], measuring the difference between instatenious current and current at the end of the pulse. Gate lag is measured pulsing from: Vgs<Vp (pinch-off voltage) with Vds>0 and is kept constant to Vgs>>Vp. Drain lag is measured pulsing from Vds=0V, while Vgs>Vp and is kept constant to Vds>>0.

While gate lag measureemts did not reveal any difference between devices from two different epi vendors, drain lag test showed that capture time constant for vendor 2 is showing larger delta between two currents and that emission time constant for vendor 2 is in order of 50 usec.

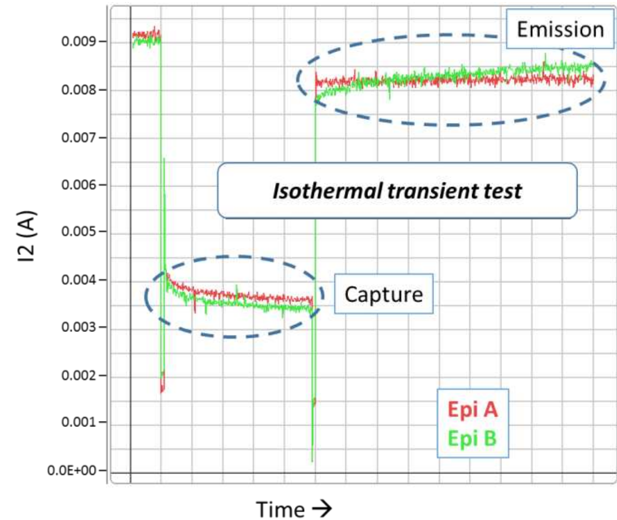

Figure 5: Transient response for test 2, isothermal transient test on two epi types

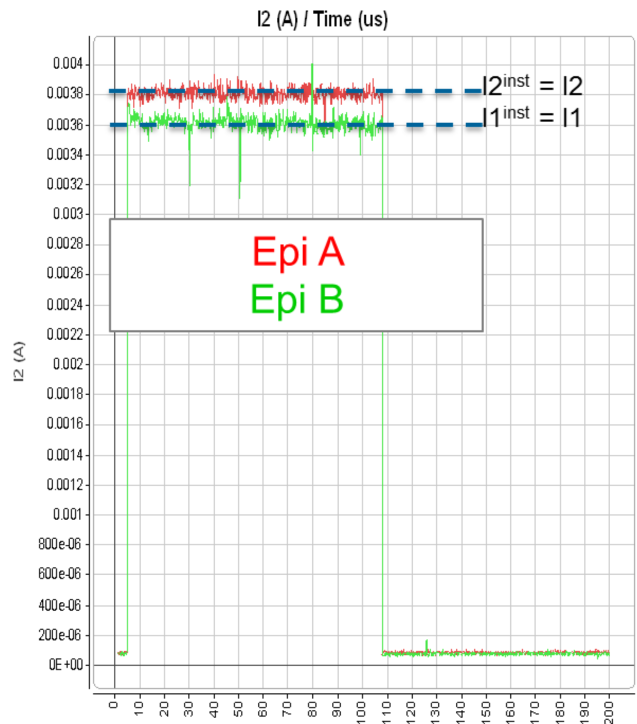

Figure 6: Transient response for test 3 (gate lag measurement), pulsing from Vgs<Vp, Vds=const. to Vgs>>Vp.

For the gate lag measurement, instantaneous drain current and current at the end of the pulse are identical:

$$\Delta I2 = I2^{inst} - I2 = 0$$
$$\Delta I1 = I1^{inst} - I1 = 0 \quad (1)$$

Drain lag measurement reveals that drain lag time constant for Epi B is larger, which means that de-trapping and trapping of carriers are longer.

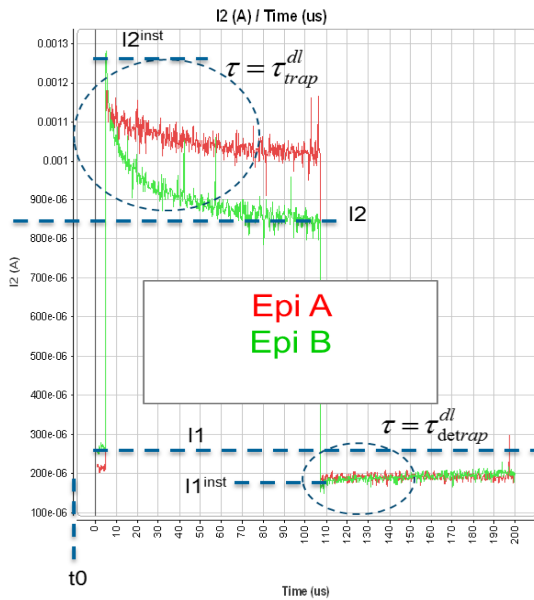

Figure 7: Transient response for test 3 (drain lag measurement), pulsing from Vds=0, Vgs>Vp to Vds>>0.

Both epi types showed that under drain lag conditions, when drain voltage was changed from high to low value, main difference is in de-trapping time constant and that device with good DEVM response is not actually "trap-free" (capture time constant was in order of 10's usec) but the release of traps took longer for epi A and thus did not impact DEVM results as the de-trapping time constants was much longer.

These measurement results helped us to connect device performance to epitaxial and substrate differences between two epi vendors. Figure 8 shows cross section of E-mode pHEMT device with ideal and actual response of drain current that was captured in transient measurement under DEVM bias conditions. Regions marked 1, 2 and 3 on drain current response versus time match depletion regions on pHEMT device cross section. Under drain lag that proved to be dominant time constant and reason for difference in time response between two epi vendors, at the beginning of the pulse, depletion region in device reaches epitaxial-layer/substrate interface. It was demonstarted in literarture [3] that difference in surface treatment and interface contamination during epi growth is related to drain lag and can have significant impact on device characteristics depending on application. In WLAN designs, shallow traps with low activation energy located at the epi-substrate interface in material from epi vendor B were correlated to poor DEVM performance.

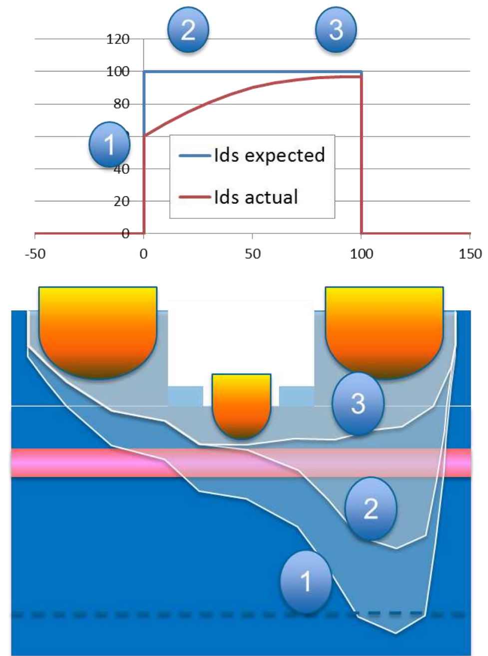

Figure 8: pHEMT cross section and corresponding depletion regions under DEVM bias conditions

The observed differences demonstrate how a simplified test can show specific areas of the device for focused improvement. Previously, SIMS, cross-sections and PCM data were the main clues for yield improvement and supplier matching. With this improved test flow, we will demonstrate that tests 1, 2 and 3 are all required for a complete understanding of the device impacts on circuit-level performance.

CONCLUSION

Transient data revealed not only the magnitude but also the mechanism for differences in drain current response under DEVM conditions. The measurement flow presented for trapping characterization can also be applied to other devices such as GaN HEMTs. Having a simple, device level method to quantify time constants for different device processes is useful not only for design but also in process and epi supplier qualification.

REFERENCES

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ACRONYMS

pHEMT: Pseudomorphic High-Electron-Mobility Transistor

DEVM: Dynamic Error Vector Magnitude

WLAN: Wireless local area network