Above 2000 V breakdown voltage on ultrathin barrier AlN/GaN-on-Silicon transistors

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Abstract

A 3-terminal breakdown voltage of 2.3 kV has been achieved on an AlN/GaN heterostructure grown on silicon (111) substrate using an optimized local substrate removal. The epitaxy was grown by metal organic chemical vapor deposition with a total buffer thickness of 5.5 µm. In order to suppress the parasitic substrate conduction phenomena under high electric field, the Si substrate has been locally etched in the high electric field region. After local substrate removal, the device breakdown voltage increased from 1.6 kV to 2.3 kV for 30 µm gate-drain distance in spite of the use of a 6.0 nm ultrathin barrier layer. The high 2DEG carrier density (2×10^{13} cm^{-2}) provided by the high polarization AlN barrier results in an extremely low specific on-resistance of 4.6 mΩ.cm^2.

INTRODUCTION

New emerging high-power applications are driving the industry to develop a new generation of power devices that can operate at above 1kV while maintaining high efficiency. GaN's wide band-gap semiconductor properties and the compatibility with silicon technology lead to high expectations in low-cost power electronics with breakthrough performance, especially for high voltage DC-DC converters. High Electron Mobility Transistors (HEMT) using AlN ultrathin barriers have already demonstrated high performances combining high breakdown voltage, high sheet charge density and high electron mobility on silicon substrate [1-3]. Indeed, this would lead to high voltage GaN HEMTs with extremely low R_{ON} as needed in order to increase the overall power device efficiency. However, this technology still suffers from the limitation of the silicon substrate since the breakdown voltage occurs at the buffer / silicon interface and generates a leakage current path when using large gate to drain spacings [4]. In order to suppress this parasitic substrate conduction, the Si substrate has been removed in the high electric field region [5].

EXPERIMENT

The AlN/GaN heterostructure were grown by metal organic chemical vapor deposition (MOCVD) on a 4 in. Si (111) substrate with a total buffer thickness of about 5.5 µm. On top of the GaN channel layer, a 6.0 nm ultrathin AlN barrier layer and a 3.0-nm-thick in situ Si_3N_4 cap layer were deposited, as shown in Fig. 1. Room-temperature Hall measurements showed high electron sheet concentration of 2×10^{13} cm^{-2} together with a mobility of 1050 $cm^2.V^{-1}.s^{-1}$ in the channel resulting in a sheet resistance (R_{sh}) of 290 Ω/□. Device processing was performed as follows: ohmic contacts were formed directly on top of the AlN barrier layer by etching the in situ Si_3N_4 layer. A Ti/Al/Ni/Au metal stack was used, followed by rapid thermal annealing at 875 °C. Device isolation was achieved by nitrogen implantation. Ohmic contact resistances (R_c) extracted from linear transmission line model (TLM) structures were 0.4 Ω.mm. A gate length of 1.5 µm was defined by e-beam lithography. Ni/Au gate metals were deposited on top of the AlN layer by carefully etching the in-situ SiN cap layer with low-power SF_6 plasma. The gate-source distance was 1.5 µm, the gate-drain spacing was varied from 5 to 30 µm and the gate extension towards the drain (field plate) was 0.75 µm. The device width was 50 µm. It has to be pointed out that no source field plates or gate dielectrics have been implemented in these devices.

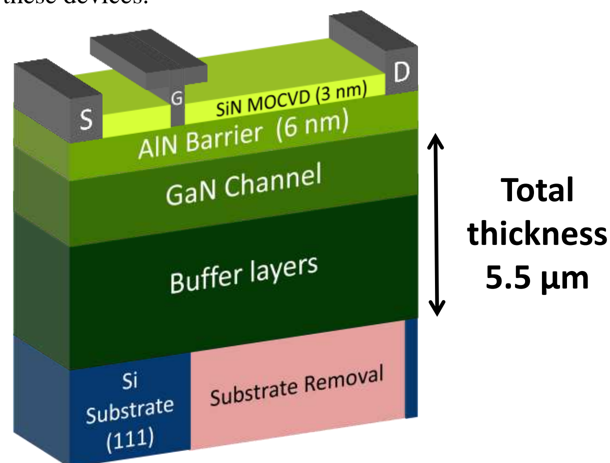

Figure 1 : Schematic cross section of the AlN/GaN structure with the local substrate removal.

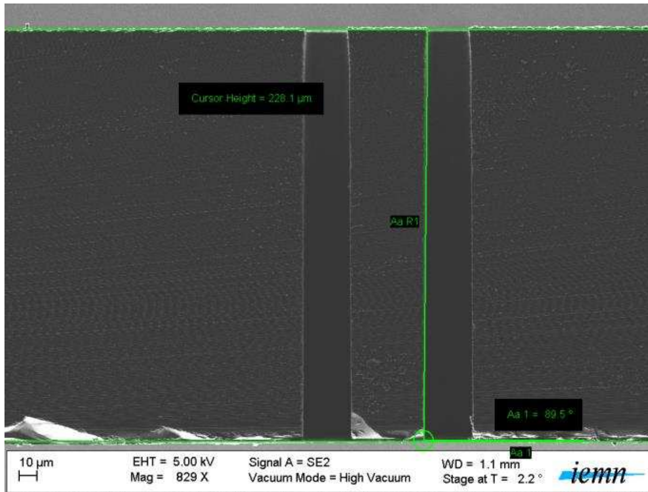

Figure 2 : SEM cross-section of the etched silicon trenches.

Once the front-side processing is completed, the Si substrate has been thinned and polished down to 200 µm. Afterwards, the Si substrate has been etched up to the buffer layer using an STS (Surface Technology Systems) deep reactive ion etching equipment based on the Bosch process all around the drain of the transistor. The Si substrate has to be etched locally and trenches design should be kept as short as possible in order to avoid a significant degradation of the thermal dissipation. In this case, the trenches covered fully the gate-drain region. This process is an alternation of passivation and etching steps leading to a highly reproducible and vertical etching with high aspect ratio (Fig 2). It is worth to note that this process is fully scalable in view of large devices using gate widths of several tenths of millimeter as needed for high power operation. The Si backside removal has been performed on half of the cells across the wafer so that a proper comparison without growth and/or process variation can be achieved.

RESULTS

DC characteristics before and after the local substrate removal of a 1.5×50 µm AlN/GaN-on-Si HEMT using a gate- drain spacing (L_{GD}) of 30 µm are shown in Fig. 3 and Fig. 4. Although the device geometry was rather large, the maximum DC output current density at V_{GS} = +2 V was as high as 0.55 A/mm before etching (see Fig. 3), as expected from the large polarization generated in the two-dimensional electron gas (2DEG). Transfer characteristics in Fig. 4 reveal an extremely low leakage current (below 0.1 µA/mm) in spite of the Schottky gate structure (no gate insulator). After the local substrate removal, the maximum current density is reduced to 0.45 A/mm which is due to the degraded thermal dissipation within the trenches as 2DEG properties remained unchanged. Consequently, the corresponding specific on-resistance increases accordingly from 4.1 mΩcm² to 4.6 mΩcm².

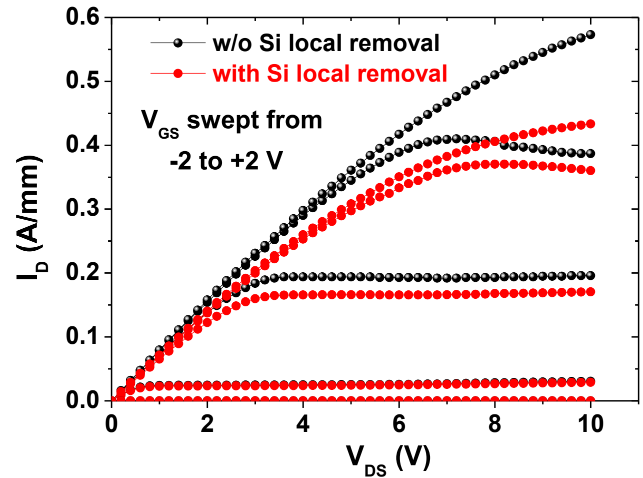

Figure 3 : I_D–V_{DS} characteristics of a 1.5×50 µm AlN/GaN-on-Si devices with L_{GD} = 30 µm before and after local substrate removal.

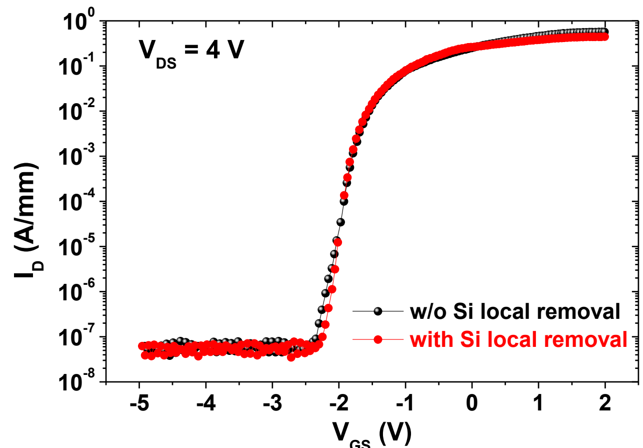

Figure 4 : Transfer characteristic of a 1.5×50 µm AlN/GaN-on-Si devices with L_{GD} = 30 µm with and without local substrate removal at V_{DS} = 4V.

Three-terminal breakdown voltage measurements have been carried out on various transistor designs at V_{GS} = -5 V (deep pinch-off). The breakdown voltage was defined as the drain-source voltage (V_{DS}) at which the drain current density (I_D) reaches 1 mA/mm. Results are represented in Fig. 5. In both cases, the device breakdown voltage increases linearly with gate-drain distances up to L_{GD} = 15 µm. For devices without local substrate removal, BV saturates around 1.6 kV, due to the parasitic conduction in the substrate. This high BV value reflects the thick buffer layers of high quality. For locally etched substrate devices, the silicon limitation is suppressed and the breakdown voltage continues to increase for larger gate-drain distances to reach 2.3 kV for L_{GD} = 30 µm. Three-terminal off-state characteristics of the 30 µm gate-to-drain spacing transistor with and without local Si removal are plotted as a function of the drain bias in Fig. 6. Without Si removal, we systematically observe the bump around 1000 V, related to the buffer/Si interface, followed by an exponential increase of the leakage current resulting in an electron avalanche and a device breakdown at 1.6 kV,

most likely due to the electron accumulation at the buffer/Si interface. On the other hand, for locally removed Si devices it must be noticed that no drain leakage current variation occurred and hard breakdown is observed at 2.3 kV confirming the absence of conductive path.

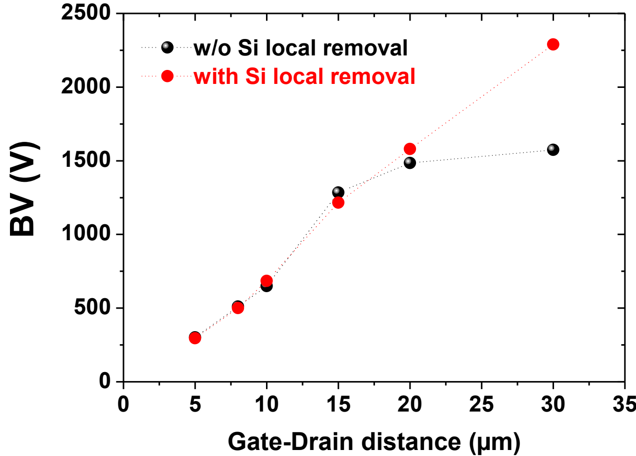

Figure 5 : Breakdown voltage as a function of the gate-drain spacing.

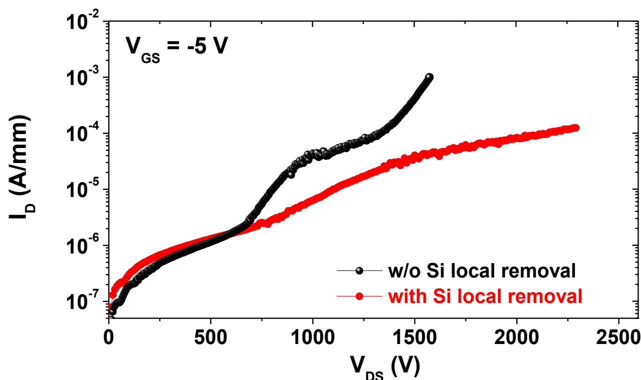

Figure 6 : Off-state characteristics of a 1.5×50 µm AlN/GaN-on-Si devices with L_{GD} = 30 µm before and after local substrate removal at V_{GS} = -5V.

The Fig. 7 represents the benchmarking of the specific on-resistance as a function of the breakdown voltage for GaN-on-Silicon transistors rated beyond 1 kV. The translated specific R_{ON} of 4.6 mΩ cm^2 combined with a BV of 2.3 kV for the devices with L_{GD} = 30 µm compares favorably with the state-of-the-art. These results establish the highest lateral breakdown voltage for GaN-on-Si devices while using an extremely high polarization ultrathin AlN barrier layer.

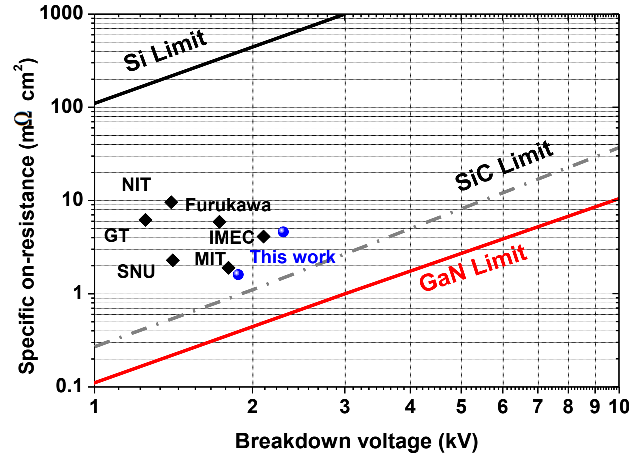

Figure 7 : Benchmarking of specific on-resistance versus BV of GaN-on-Si transistors rated beyond 1 kV.

CONCLUSIONS

We have successfully fabricated extremely high-voltage AlN/GaN-on-Si HEMTs with a buffer thickness 5.5 µm, despite a very high 2DEG carrier density of 2×10^{13} cm^{-2}. A local substrate removal has been realized around the drain in order to eliminate the electron accumulation at the buffer/Si interface which allows a drastic improvement of the device breakdown voltage. A three-terminal breakdown voltage of 2.3 kV combined with a specific R_{ON} of 4.6 mΩ cm^2 were achieved for a gate-drain distance of 30 µm. Breakdown voltage could be improved by adding multiple field-plates and a dielectric under the gate in order to avoid gate premature degradation under such high electric fields. Also, an AlN thick layer (8 to 10 µm) delivering high breakdown field (> 4 MV/cm) followed by a Cupper metallization will be deposited inside the trenches to significantly improve the thermal dissipation without degrading the outstanding breakdown voltage.

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