0.18 μm E/D-mode pHEMT using I-line Photolithography for Microwave Application

Min-Li Chou[1], Yi-Shun Lin[2], Ming-Tai Wu[2], Sheng-Chun Wang[2], Hsin-Chi Wang[2], Li-Chung Lee[2], Zhi-Peng Lin[2], Chih-Yu Tseng[2], Fred CH Lin[2], Pang-Shao Chen[2], Houng-Chi Wei[2], Chian_Gau[1], Shih[1] and Hsien-Chin Chiu[1]

[1]Department of Electronic Engineering, Chang Gung University, No. 259, Wenhua 1st Rd., Guishan Dist, Taoyuan, Taiwan.
E-mail: d0127101@stmail.cgu.edu.tw, Tel: +886-3-2118800 ext.: 3645.
[2]Wavetek Microelectronics Corporation, No. 10, Innovation 1st Rd., Hsinchu Science Park, Hsinchu, Taiwan.
E-mail: hc_wei@wtkmicro.com, Tel: +886-3-5782259 ext.: 22815.

Keywords: E/D-mode, pHEMT, I-line photolithography, LNA, microwave application

Abstract

A high performance 0.18 μm E/D-mode pHEMT using manufacturable cost-effective I-line stepper photolithography technology is described in this paper. Its E-mode pHEMT exhibits an available gain of 13.9 ± 0.93 dB and noise figure of 0.298 ± 0.028 dB at 6 GHz. Using this technology, a wideband LNA MMIC with the 3-dB bandwidth from 4.2 GHz to 7.5 GHz, and the minimum noise figure of 0.8 dB has been demonstrated. This high performance validates its effectiveness in microwave applications.

INTRODUCTION

Low-voltage and low power consumption are the important performance in microwave applications. The monolithically integrated enhancement- and depletion-mode (E/D-mode) pseudomorphic high electron-mobility transistor (pHEMT) on GaAs technology have been developed for high-speed or high frequency RF communication systems. Microwave integrated circuits obtain several advantages from such an E/D-mode technology compared to conventional D-mode only technology [1, 2]. For switch needed model, the D-mode transistor can be used for switch and E-mode transistor for a logic circuit for saving control lines. It can be easily integrated into different sub-circuits, reduce the number of chips and also reduce manufacturing cost.

The deep sub-micron pHEMT process provides high frequency, high efficiency and output power performance. Most lithography technologies using e-beam lithography can achieve to high unit selling price, low yield and variable performance. However, direct e-beam write is relatively slower and more costly than optical stepper. This paper reports the development of a 0.18 μm E/D-mode pHEMT manufactured using cost-effective I-line stepper photolithography with reliable shrinkage process. The RF characteristic note that the E-mode pHEMT device has good high frequency performance. In order to consider high frequency for MMIC design, the wideband and low power consumption LNA are also presented in this paper.

DEVICE RF CHARACTERISTICS

A high performance 0.18 μm gate length E/D-mode pHEMT MMIC has been demonstrated using manufacturable cost-effective I-line stepper photolithography with reliable shrinkage process. Figure 1 shows the SEM cross-section picture of this 0.18 μm E-mode pHEMT.

Figure 1 0.18 μm T-gate profile on E-mode pHEMT

The performance of 8 × 50 μm E-mode pHEMT device is shown in Figure 2 and Figure 3. Figure 2 shows the variable gain and noise figure under V_{DS} = 3.0 V and V_{GS} = 0.45 V bias conditions. The data was collected from five sites of the wafer. The available gain is 13.9 ± 0.93 dB and noise figure is 0.298 ± 0.028 dB at 6 GHz. Linearity performance with biasing V_{DS} = 4 V and V_{DS} = 5 V is shown in Figure 3. The measured large signal gain is about 16 dB and OIP3 is about 35 dBm. Device specifications are shown in Table 1.

The proposed process can be applied to microwave applications including low-noise amplifiers, power amplifiers, etc. The bias circuit for communication products would be less complicated.

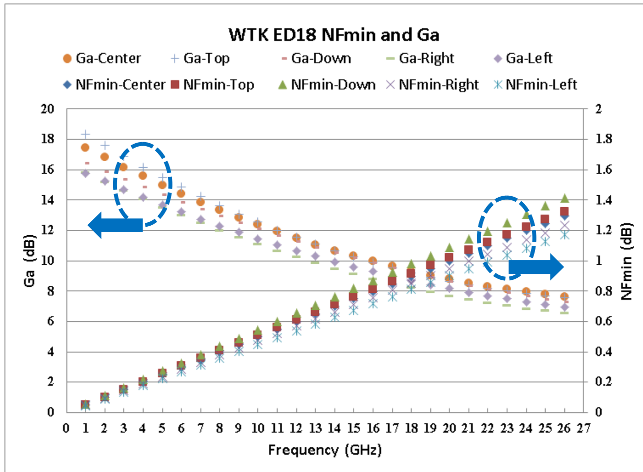

Figure 2 Measurement results of associated gain and minimum noise figure.

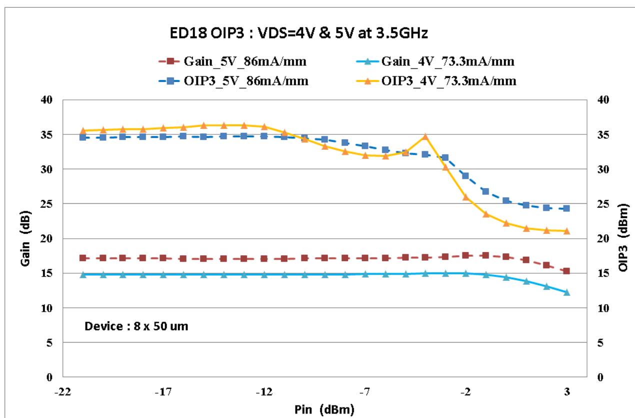

Figure 3 Measurement results of large signal gain and OIP3.

TABLE I

DEVICE SPECIFICATION OF 0.18 µM ED-MODE PHEMT

	E-Mode Device (0.18 µm)			D-Mode Device (0.5 µm)		
Parameter	Target	LSL	USL	Target	LSL	USL
V_{th}/V_p (V)	0.3	0.2	0.4	-1	-1.2	-0.8
I_{dss} (mA/mm)	1.0E-04	-	0.1	300	240	360
Gm_{max} (mS/mm)	850	750	950	350	280	420
Id_{max} (mA/mm)	450	360	-	450	360	-
BV_{gd} (V)	12	8	-	16	12	-
R_{on} (Ohm-mm)	1.2	-	2.0	1.0	-	1.5
f_T (GHz)	90	-	-	33	-	-
f_{Max} (GHz)	140	-	-	90	-	-

DESIGN OF LNA

The wideband and low power consumption cascade LNA circuit was implemented with the Wavetek's 0.18 µm E/D-mode pHEMT process and its schematic is presented in Figure 4. The chip photograph is shown in Figure 5 with a total chip size of 0.43 mm^2, and the gate width for M1~M2 are 6 × 25 µm and 6 × 50 µm, respectively. Under a 3.3 V supply voltage, the dc power consumption of the LNA is 26.4 mW. The S-parameters were measured using on-wafer measurement. As show in Figure 6, the amplifier has 3-dB frequency bandwidth of 3.3 GHz with peak gain of 19.6 dB at 5.95 GHz. A gain flatness of ± 1 dB is achieved in the wide range from 4.95 to 7.42 GHz. The noise performance is shown in Figure 7. The average noise figure in 5 ~ 6.5 GHz band is 1.15 dB with a minimum of about 0.8 dB. This LNA also has presented its high performance in 802.11ac/n WLANs communication systems for **Wavetek's 0.18 µm E/D-mode technology.**

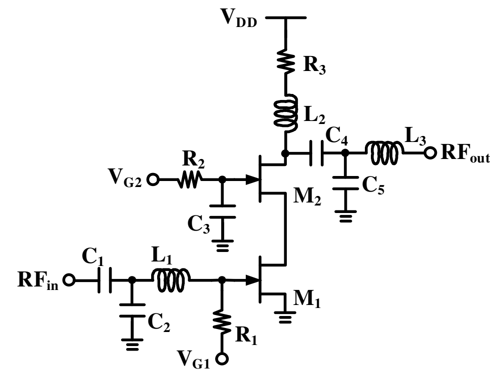

Figure 4 Schematic of LNA Design.

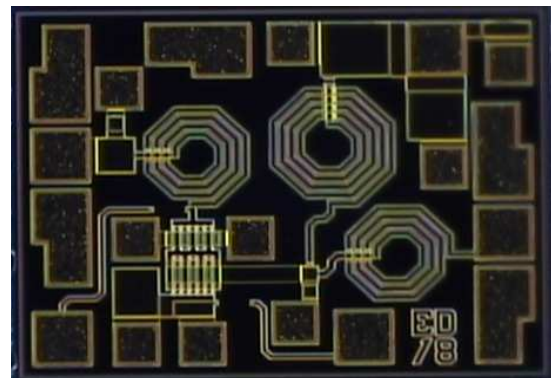

Figure 5 Microphotograph of LNA.

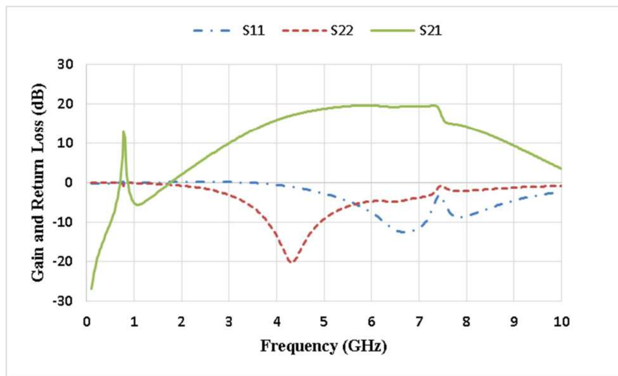

Figure 6 Measurement results gain and return loss.

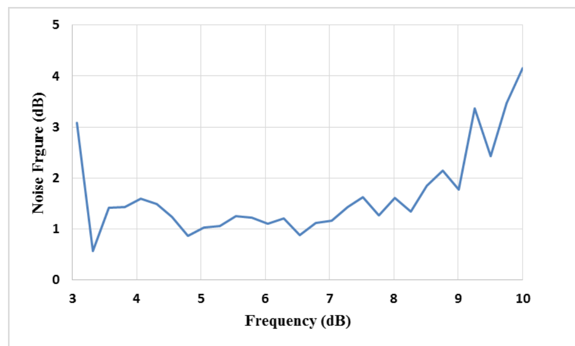

Figure 7 Measurement results of noise figure.

Conclusions

We have presented Wavetek's 0.18 µm E/D-mode pHEMT technology by I-line stepper photolithography for microwave applications. The available gain and minimum noise figure at 6 GHz for an 8 × 50 µm E-mode pHEMT device are 13.9 ± 0.93 dB and 0.298 ± 0.028 dB, respectively. A wideband LNA with **the 3-dB bandwidth of 3.3 GHz, and the minimum noise figure of 0.8,** has also demonstrated its feasibility in MMIC applications.

References

[1] D. C. Dumka, H. Q. Tserng, M. Y. Kao, E. A. Beam and P. Saunier, "High performance double-recessed enhancement –mode metamorphic HEMTs on 4-InGaAs substrate," *IEEE Electronic Device Lett.*, Vol. 24, No. 3 pp. 135-137, March 2003.

[2] Y. Bito, N. Iwata and M. Tomita., "64 % efficiency enhancement-mode power heterojunction FET for 3.5 V Li-ion battery operated personal digital cellular phones," *IEEE MTT-S Tech. Digests*, pp. 439-42, 1998.