Commercialization of Millimeter-Wave Semiconductors for 5G – A Unique View from Test & Measurement

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Abstract

5G poses big new questions for the role of semiconductors in electronics. Exponential growth in users, data, and applications are driving wider channel bandwidths, lower latency, higher density, and greater mobility. To achieve these goals, 5G will move from RF to millimeter-wave frequencies, long the domain of aerospace and defense applications. The economics of commercial 5G will be the same as past generations – very low costs at very high volumes – thus favoring semiconductors based on silicon. On the other hand, performance goals of many millimeter-wave A/D systems favor III-V compound semiconductors. So, which technologies will play major roles in 5G? The question is unanswered today, but unique insight may be gained from test and measurement which serves both the commercial and A/D electronics markets.

INTRODUCTION

The exponential evolution of cellular technology truly has been remarkable, encompassing four technology generations to date: from analog voice (1G) of the 1980s, digital voice (2G) in the 1990s, digital voice and data (3G) in the 2000s, and today's generation (4G) that delivers full mobile internet. Work on tomorrow's fifth generation (5G) technology has started and promises to deliver ubiquitous connectivity, not just to everyone, but to everything. The vision of the 2020s and beyond is nothing short of revolutionary:

- 100× faster data rates to support the growth in data
- 100× higher efficiency for machine-type communications enabling the Internet of Things
- 99.999% reliability and <1ms latency in mission-critical use cases
- 1000× higher capacity and 100× higher density to handle the explosion of connected devices

New mobile and fixed radio architectures are needed to fulfill this vision. Both will maximize spectral efficiency and spatial diversity by using complex modulation, channel bonding and carrier aggregation, antenna beam-forming, and multiple-input multiple-output (MIMO) techniques. Furthermore, the RF spectrum is full, and new cellular band allocations will be needed in the microwave and millimeter-wave spectrum. Governments worldwide are considering shared allocations for mobile wireless in many frequency bands between 15 and 50GHz, with interest currently centered on 28 and 39GHz, expanded access in unlicensed bands at 60GHz for fixed wireless, and bands between 70 and 95GHz for cellular backhaul. 5G will commercialize microwave.

Aerospace and defense (A/D) markets are similarly evolving. Signal monitoring applications acquire very wide segments of spectrum and, simultaneously, identify and track specific signals of interest in a forest of interference. Electronic warfare systems demand gapless capture, low-latency real-time signal processing, and streaming playback of wide-bandwidth signals. Ultra-low oscillator phase noise is required to increase the sensitivity and extend the range of radar systems. Most A/D systems are now implemented with multiple distributed apertures to increase performance and capability. And across the entire A/D application space, the need for broadband coverage of the frequency spectrum from near-dc through W-band (110GHz) has been a constant. A/D markets want wider frequency coverage, higher dynamic range, and everything done faster.

The test and measurement (T&M) market, serving both commercial and A/D markets, has a unique vantage point in this evolution. The T&M market is subject to similar and parallel trends: high performance implies accurate and precise measurements; low cost implies low cost of test. T&M products participate in the entire life cycle of any electronic system, with high-performance general-purpose instruments valuable in early research and product development, more specific market-focused solutions desirable for design validation and standards compliance, to low-cost high-throughput instruments required in volume manufacturing. And the T&M industry plays important roles in the development of new technologies and standards. This plenary will discuss how these emerging market forces will impact both T&M solutions and the underlying semiconductor and assembly technologies that will be critical to meeting the performance and cost goals these markets demand.

TEST & MEASUREMENT SOLUTIONS

By all measures, these market forces pose daunting challenges for engineers developing 5G, A/D, and T&M

electronics. Yet in T&M, these seemingly diverse vectors act in much more similar directions than one might expect. The first direction should be obvious – higher performance, measured by the quality of analog signal processing and the breadth and depth of digital signal processing. While traditional metrics such as output power, noise floor, and dynamic range continue to be important, new system-level metrics such as error vector magnitude (EVM) and adjacent-channel power ratio (ACPR) are even more critical. Key new system attributes include coherency among many channels and real-time signal analysis and generation.

A second direction is a radical shift in form. Traditional frequency-domain instruments – signal analyzers, signal generators, and vector network analyzers – are evolving into new forms: real-time coherent transceivers (RCT) and vector component analyzers (VCA). Remote heads increase performance by separating the front end from the rest of the measurement hardware. Dissipated power and size are becoming equal in importance to performance. The future will be defined by scalability, flexibility, and density. A catalog of instruments in multiple form factors, from the traditional bench top to the small measurement transducer connected to the cloud, will be required for the broadest market reach.

A third direction is a significant evolution in connectivity. Two separate trends are important here. Over-the-air (OTA) testing will be required for a growing number of electronic systems that lack conductive connections – connectors or on-wafer pads – at the RF interfaces. New measurement hardware will include an antenna to enable radiative connections, and new calibration strategies must be invented and implemented to move the measurement plane to the antenna in the device under test. The other trend is data transfer among the different T&M hardware elements and between the hardware and external computing resources, including the cloud. Tomorrow's instruments need fast and wide data pipes and a set of defined interfaces for efficient interoperability.

The final direction is cost of test. T&M hardware should reflect the market expectations of price/performance curves. T&M software should deliver market-valued measurement science and data analytics while optimizing ease of use and minimizing time to result. Overall, the cost of test needs to match market needs.

Just as 5G will be revolutionary, T&M is undergoing its own revolution of sorts – today's paradigms are necessary but not sufficient to meet tomorrow's measurement needs. To realize the vision shown in Fig. 1, a broad range of state-of-the-art semiconductor and assembly technologies will be needed.

Fig. 1. The future of T&M solutions

Semiconductor Technologies

A wide array of semiconductor technology options exist today. For electronic integrated circuits (ICs), the different options are commonly described by the semiconductor material system and transistor type. Material systems include silicon (Si), by far the most common, and three compound semiconductors: gallium arsenide (GaAs), gallium nitride (GaN), and indium phosphide (InP). The transistor type is either field-effect (FET) or hetero-junction bipolar (HBT), the modern form of a bipolar junction transistor. For the purpose of technology selection, however, further simplification is useful, to just three technology categories:

- CMOS: Si-based complementary metal-oxide-semiconductor FETs
- SiGe BiCMOS: a combination of silicon-germanium (SiGe) HBTs and CMOS
- III-V: GaAs, GaN, and InP FETs and HBTs

Ultimately, the selection is determined by performance requirements and the economics of the end market. Fig. 2 diagrams, in a very general way, the relationships among the three technology categories with respect to two key attributes: performance and integration, as well as development and manufacturing costs. A few points are worth considering. Digital applications are almost entirely addressed with CMOS, with SiGe and III-V participating only at the highest performance levels. Analog applications are served by all three categories, with SiGe and III-V addressing a large range of performance levels, with CMOS below. In both types, SiGe and III-V are primarily differentiated by the level of integration: SiGe, built on top of a CMOS infrastructure, can support a higher level than III-V.

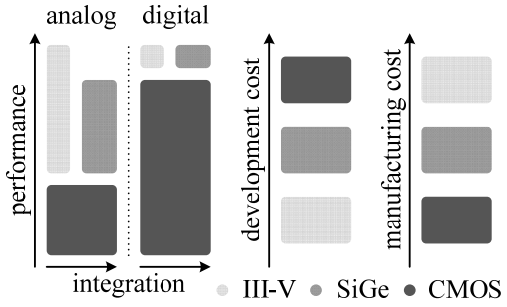


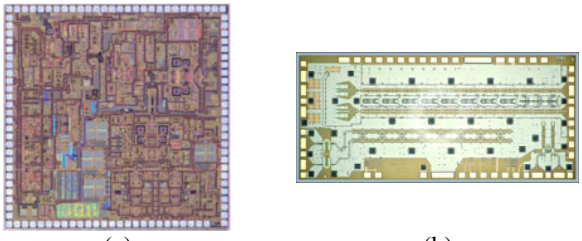
Fig. 2. Relationships among CMOS, SiGe, and III-V.

The economics of commercial markets – generally, very high volume, performance that complies with published technical standards, and lowest part cost – overwhelmingly favor CMOS. Other semiconductor technologies are considered only when a CMOS-based solution does not exist. A few examples include SiGe transceivers in automotive radar systems, GaAs amplifiers in mobile telephones, and GaN power amplifiers in cellular base stations. Emerging

commercial 5G requirements, however, represent a large disruptor, potentially opening new opportunities for non-CMOS technologies.

The economics of T&M and A/D markets are very different. Volume requirements are many orders of magnitude lower, and cost-performance curves are much more elastic. Development cost plays a large role in the selection process, and mask costs can be a significant fraction of that cost. Very approximately, mask charges are $10k to $50k for III-V, $100k to $500k for SiGe, and $1M to $5M for CMOS. In these markets, extremely high development costs make CMOS suitable only for a very few large, generic, digital needs, such as data conversion and digital signal processing. Many hardware platforms, each addressing a particular application and set of requirements, leverage a single, large IC investment.

On a smaller scale, the same forces are at play in the selection of SiGe and III-V for analog needs. At the highest performance levels, III-V is the only choice. On the other hand, SiGe has a clear advantage in the integration of analog functions with digital control and processing. Development costs again play a significant role. SiGe is attractive for applications that need higher levels of integration and can amortize the development cost over relatively larger volumes, a constraint that is irrelevant for high-volume commercial markets. In fact, a very wide variety of SiGe and III-V ICs comprise RF front ends inside Keysight's microwave and millimeter-wave instruments. Photographs of recent Keysight ICs are shown in Fig. 3.



(a) (b)

Fig. 3. Examples of recent Keysight (a) SiGe and (b) InP ICs.

Each III-V technology generally satisfies a specific need: for example, GaN FETs for highest output power, InP FETs for lowest noise figure, or GaAs FETs for control. The use of GaAs HBTs has been more widespread than other III-V semiconductor technologies across multiple markets. This was certainly true at Keysight in the past, but today's workhorse is the InP HBT.

SiGe and InP HBTs have a lot in common, so a side-by-side comparison is useful. Table I compares relevant metrics for various state-of-the-art processes. Keysight released its first-generation InP process in 2007 [1,2] and a second generation in 2016 [3]. InP HBTs have a unique combination of attributes that make them attractive for T&M applications. InP speed, as measured by the traditional f_T and f_{MAX} frequency figures of merit and CML gate delay, compares favorably with SiGe, yet InP has 4× higher breakdown voltage. This combination of high speed and breakdown enables tremendous flexibility in addressing the requirements of multiple applications with a single design. InP integration levels, while lower than SiGe, cover most T&M needs. Finally, InP reliability has been demonstrated [3] using the same robust techniques that Keysight previously applied to GaAs HBTs [4]. This provides the freedom to combine multiple InP ICs into complex instrument-grade systems that contain many thousands of transistors.

TABLE I
COMPARISON OF INP AND SIGE

process	f_T (GHz)	f_{MAX} (GHz)	delay (ps)	BVceo (V)
Keysight 1st-gen InP	205	245	4.48	8.1
IHP DOTFIVE [5]	300	500	2.05	1.7
Keysight 2nd-gen InP	280	580	2.03	7.25
IHP DOTSEVEN [6]	520	700	1.34	1.6

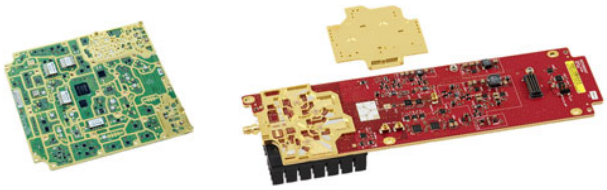
An important element in optimizing the tradeoff between performance and cost is the ability to choose the 'right junction for the function.' The breadth of semiconductor technologies available today provides a wide variety of possible options. Market forces can strongly influence the selection process. At least for T&M and Keysight, the right choices are a healthy combination of III-V for a large fraction of analog applications, a majority of which is InP HBT, SiGe for highly integrated analog and very high-performance digital, and CMOS for the largest digital needs.

ASSEMBLY TECHNOLOGIES

Assembly technologies connect semiconductor dies together to form a system and expose the functionality of the system to the world. For several decades now, the inconsistency in the geometries of dies, measured in um, and assemblies, measured in mm, has necessitated the use of various package technologies as interposers, resulting in the ubiquitous 'plastic IC package.' The vast majority of electronic assemblies today consist of semiconductor dies of all flavors packaged in a plastic surface-mount technology (SMT) and attached to a printed circuit-board assembly (PCA). T&M use of SMT PCAs parallels the overall industry, with specific intellectual property focusing on package lead-frame and circuit-board footprint designs to extend the operating frequency of plastic packages. Fig 4a is a picture of the analog front end of a microwave analyzer. Density is lower than, for example, PCAs in mobile telephones, primarily due to transmission lines and filters embedded in the PCA and the need for shields. The maximum operating frequency of this PCA is ~10× higher than a mobile telephone.

SMT PCA technologies, however, fail for the highest-performance systems and at millimeter-wave frequencies due to relatively poor material properties, uncontrolled electrical transitions, and imperfect shielding. For these applications,

significant in both T&M and A/D, a decidedly different approach is taken – semiconductor dies directly attached to a mechanical carrier, interconnected with planar thin-film transmission lines, and embedded inside electrically cut-off waveguide channels. Historically the carrier has been machined out of metal; these assemblies are known as 'gold bricks.' Fig. 4b is a picture of an oscilloscope front end with a less expensive chip-on-board (CoB) approach developed at Keysight that uses the PCA as the carrier and patterned metal waveguide cavities.



(a) (b)

Fig. 4. Keysight analog front ends: (a) analyzer and (b) oscilloscope.

Two significant trends have emerged to satisfy the ever-present demand for higher functionality in smaller size and at lower cost. System-on-chip (SoC) approaches integrate multiple functions on a single die. These are ideal for complex systems implemented entirely in CMOS or SiGe, and many examples in many markets exist. Alternately, system-in-package (SiP) approaches integrate multiple dies inside a single package. Dense systems can be created, especially when combined with chip-stacking technologies. Analog performance is still limited by the package technology, but continual improvements, for example advances in fan-out wafer-level packaging (FOWLP), continue to push operating frequencies toward millimeter-wave.

The best technology, especially for T&M, is a marriage of these two approaches. Desirable attributes include:

- the elimination of the package
- heterogeneous integration of die of any size or substrate
- high-density and high-frequency inputs and outputs
- true three-dimensional routing
- batch fabrication and assembly

Such assembly technologies would deliver the highest performance in the smallest size at the lowest cost. PolyStrata® from Nuvotronics, Inc. [7] is a prime example that meets many of these criteria. The DARPA CHIPS (Common Heterogeneous Integration and Intellectual Property Reuse Strategy) Program [8] is another possible direction worth monitoring. It seeks to create an infrastructure in which reusable IP blocks called 'chiplets' can be interconnected with a set of defined interfaces and assembled into complete systems on an interposer very quickly and cheaply.

Conclusions

5G and A/D market trends continue to push the boundaries, and semiconductor and assembly technologies must continually evolve to keep pace. While differences in market economics may drive different technology choices, ever-evolving market requirements will continue to open new opportunities. T&M markets will evolve in parallel, making use of the widest range of technology options to meet customer's increasingly high expectations for performance while also meeting customers' aggressive cost of test goals.

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[7] www.nuvotronics.com

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Acronyms

5G: fifth generation (cellular wireless)
A/D: aerospace and defense
CMOS: complementary metal-oxide-semiconductor
FOWLP: fan-out wafer-level package
FET: field-effect transistor
GaAs: gallium arsenide
GaN: gallium nitride
HBT: hetero-junction bipolar transistor
IC: integrated circuit
InP: indium phosphide
OTA: over the air
PCA: printed circuit-board assembly
Si: silicon
SiGe: silicon-germanium
SiP: system-in-package
SMT: surface-mount technology
SoC: system-on-chip
T&M: test and measurement