Current Progress in SiC Power MOSFETs and Materials

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Abstract

The introduction of SiC power MOSFETs has enabled power systems to reduce size, weight, and cost. The latest Generation 3 MOSFETs from Wolfspeed have allowed further improvements in cost and performance. The results of Gen 3 MOSFETs in terms of avalanche ruggedness are presented. Further improvement in cost structure is being enabled by the transition to 150 mm diameter SiC substrates and epitaxy, and eventually 200 mm diameter SiC. Reductions in defect densities allow further cost reduction through improved yields.

INTRODUCTION

The integration of silicon carbide power devices into many commercial applications over the last several years [1, 2] has been driven by superior device and system performance enabled by the favorable physical properties of silicon carbide. These demonstrations have led to a wider adoption of SiC based devices into many applications, driving substantial commercial growth and maturation of the technology. This maturation is visible in three ways. First, there is an accelerating drive to increase the quality of the SiC material by reducing defects that limit yield and performance, such as micropipes and dislocations. Reducing these defects insures that manufacturers can get a high yield of high performance devices from each wafer processed. Secondly, there is the continuing drive to increase the diameter of the wafers to gain the efficiencies of scaling and reduce cost. Third, there is the drive to improve MOSFET design and processing to reduce die size and cost, increase performance, and improve the ruggedness and reliability of the devices.

SILICON CARBIDE MATERIALS ADVANCEMENTS

Wolfspeed, as the largest volume SiC substrate producer, is aggressively driving the continued advancement of SiC technology by improving the quality and increasing the size of commercial SiC wafers as is demonstrated in Fig. 1. Within efforts to reduce the defect densities in SiC substrates, the most damaging defects receive the most attention. As the density of micropipes in SiC crystals has been reduced to negligible levels, the quality improvement focus has shifted to dislocations. SiC crystals exhibit several dislocation types including basal plane dislocations (BPDs), threading edge dislocations (TEDs) and threading screw dislocations (TSDs). Specifically, the BPD has been associated with increasing the number of defects observed in epitaxy [3] and as the root cause of V_F drift in bipolar devices [4]. Leveraging rapid feedback of etch-based defect measurements, the BPD densities have been significantly reduced and substrates with very low BPD densities are now available. With subsequent epitaxial technology, the BPDs are further reduced in our epilayers to essentially zero through their conversion to relatively benign TEDs, as shown in Fig. 2 [5]. Similar to BPDs, effective and automated characterization techniques for rapid feedback to crystal growth processes were utilized to reduce the TSD density in SiC substrates [6]. Whole wafer, etch based dislocation maps demonstrating an average TSD density of 227 cm^{-2} on 150 mm substrates have been achieved. These improvements have allowed current SiC substrates to be used in highly robust, commercial devices.

We combine these substrate advancements with high quality 150 mm epitaxy to further drive the cost reduction and acceptance of SiC devices. Currently, our large 6x150 mm capacity warm-wall epitaxy reactors are efficient for growing large quantities of epitaxial layers for low to medium-voltage (300-3000V) devices and our new 8x150 mm platform demonstrates comparable properties. Our 3x150 mm horizontal hot-wall configuration takes advantage of larger area substrates while achieving increased

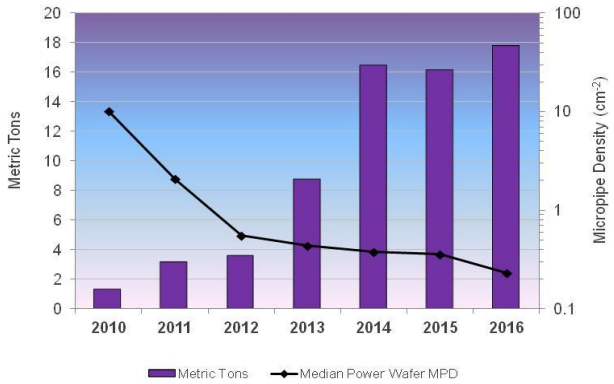

Fig. 1. Volume and quality of 150mm product over time.

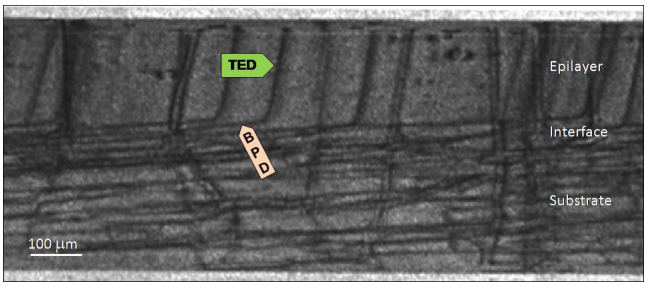

Fig. 2. Cross-sectional x-ray imagery showing the conversion of substrate BPDs into threading edge dislocations during SiC homoepitaxy.

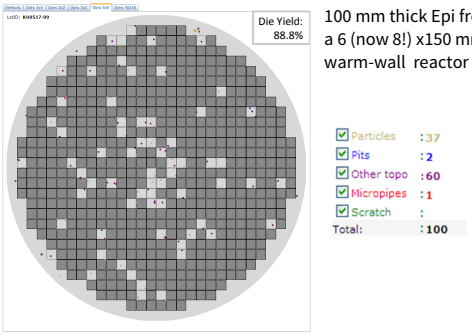

Fig. 3. 100 µm thick epitaxy growths in high throughput platforms show low defect counts.

throughput of 10kV-class epitaxial layers. Our current capability for epitaxial layer properties from both platforms and up to 100 microns thickness can be summarized as follows: The median intra-wafer thickness and doping uniformity (σ/mean) for the 3x150 mm reactor are 0.9% and 6.10%, respectively. The intra-run thickness and doping variation are 0.18% and 1.01%. The projected 5x5 mm useable area for layers of nominal 5 to 30 µm thickness for all the reactor configurations (as measured by a Candela CS2 optical surface analyzer) are approximately 92%, corresponding to an effective defect density of about 0.35 cm^{-2}, as shown in Fig. 3. [7].

For the next step in cost reduction, Wolfspeed has demonstrated 200 mm diameter SiC substrates, as shown in Fig 4 [7]. These substrates are showing micropipe densities less than 1 cm^{-2} despite the early stage of development they are in. The thickness for these substrates is 500 µm. We have also demonstrated SiC epitaxial growth on these 200 mm substrates, with thickness and doping uniformity σ/mean values of 2.2% and 1.9 %, respectively. These are already very good values, but more work is required in both bulk growth and epitaxy to bring the cost structure down to equivalency with 150 mm materials in terms of cost per cm^2.

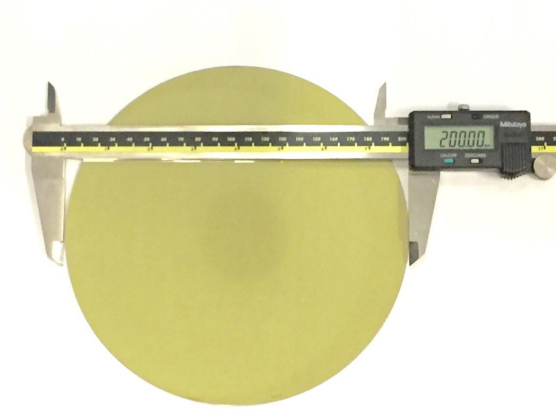

Fig. 4. 200 mm diameter SiC substrate, 500 µm thickness.

THIRD GENERATION SIC MOSFET PERFORMANCE AND RUGGEDNESS

Since the first introduction of Wolfspeed's First Generation 1200V SiC MOSFET in 2011, there has been a tremendous emphasis on refining device design and processing capabilities to continually improve their performance and reliability. In the subsequent years, Wolfspeed introduced a second generation 1200V SiC MOSFET in 2013 and a third generation 900V SiC MOSFET in 2015. Most recently in 2017, Wolfspeed released a third generation 1200V SiC MOSFET. These iterations in design and volume adoption have driven the price of SiC MOSFETs down by an order of magnitude. Through elegant iterations in device design and the proper investigation of the correlations between device design, processing capabilities, device performance and reliability, we have achieved a reduction in specific on-resistance ($R_{on,sp}$) at 25°C from 8.0 mΩ.cm^2 to 3.3 mΩ.cm^2 over the course of three generations of SiC MOSFETs. Figure 5 shows the progression in $R_{on,sp}$ at 25°C and 150°C for the three generations of 1200V SiC MOSFETs. Performance at elevated temperatures is most critical for benchmarking of power switches, and $R_{on,sp}$ of the Gen 3 MOSFET has been halved compared to the Gen 2 MOSFET at a junction temperature of 150°C.

The IV characteristics of a third generation 16 mΩ/1200V SiC MOSFET with applied V_{GS} of 15V is shown in Fig. 6. Included for comparison in Fig. 6 is the IV curve from a comparably-rated Si IGBT [8], showing the advantages of the SiC MOSFET, since it does not suffer from the built-in potential knee voltage of the Si IGBT. Fig. 7 shows the On-State Resistance ($R_{DS,on}$) as a function of temperature for the recently released 75 mΩ/1200V third generation MOSFET compared to that of an 80 mΩ/1200V second generation MOSFET.

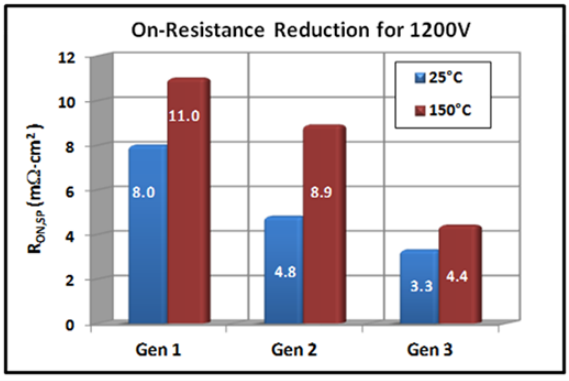

Fig. 5. Progression in the reduction of specific on-resistance ($R_{on,sp}$) of Cree's 1200V SiC MOSFETs by Generation.

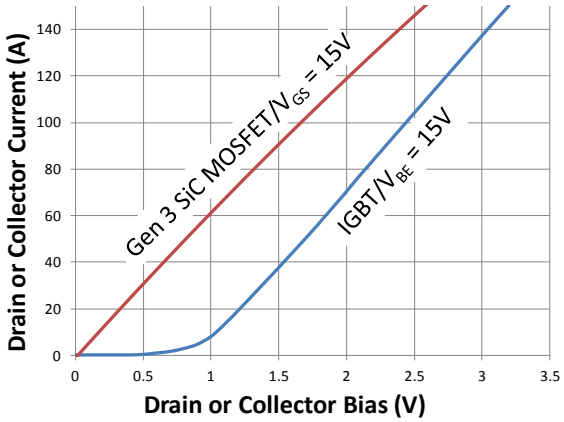

Fig. 6. IV Performance of a Gen 3 16 mΩ 1200V SiC MOSFET compared to a comparably-rated Si IGBT.

Following the commercial release of the C3M0065090D 900V-rated, 65 mΩ SiC MOSFET [9] in 2015, a much larger chip size has been released in 2017, resulting in a commercial record-low 10 mΩ/900V SiC MOSFET [10]. These large area SiC MOSFETs are optimized for applications like Electric Vehicle (EV) drive trains and other motor drive applications, because they can offer reduced on-state losses compared to IGBTs, especially at light loads, and can provide extra voltage overhead in the off-state with little to no penalty in on-state performance. Figure 8(a), shows the breakdown IV curves of a typical 10mΩ/900V SiC MOSFET, avalanching between 1100 and 1150°C, depending on the temperature. The range of breakdown voltages (V_{BRDSS}) for all parts as a function of temperature are shown in Fig. 8(b), with avalanche breakdown increasing by about 3% with a temperature increase from -55°C to 175°C.

Beyond simply demonstrating consistent V_{BRDSS} in the 900V Family of Gen 3 SiC MOSFETs, we have also proven that the MOSFETs are robust when taken into avalanche breakdown at high currents, such as during unclamped

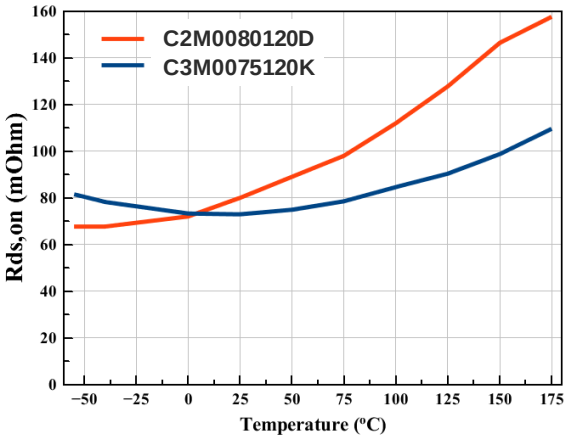

Fig. 7. $R_{DS,on}$ as a function of temperature for a second generation 80 mΩ/1200V SiC MOSFET (C2M-0080120D) compared to that of a third generation 75 mΩ/1200V SiC MOSFET (C3M0075120D).

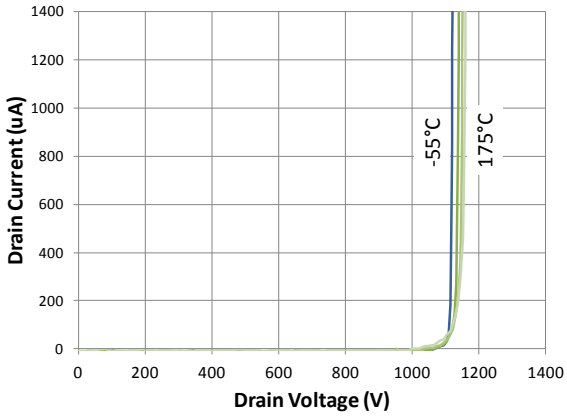

Fig. 8(a). Avalanche breakdown IV curves for a 10mΩ/900V MOSFET at -55°C, 25°C, 100°C and 175°C.

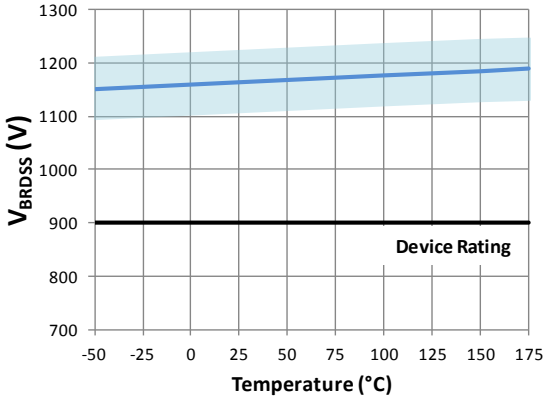

Fig 8(b). Avalanche breakdown as a function of temperature for 10mΩ/900V MOSFETs. Top line in plot indicates typical part, with the range of all parts indicated by the shading.

inductive switching (UIS), in which a MOSFET that is carrying a given current in the on-state is switched into the off-state with an unclamped inductive load that forces the MOSFET into avalanche for a period of time in order to dissipate the current that is flowing through a series inductance. Fig. 9 shows typical UIS waveforms for a 65mΩ/900V MOSFET, with a current ramp to 5A and an avalanche voltage of 1405V, which is maintained for 68.4µs once the MOSFET is switched off. In order demonstrate the ruggedness of these MOSFETs under single pulse UIS stressing, a selection of MOSFETs were subjected to UIS stresses, stepping up the dissipated energy until failure was observed. Then, a safe operating area (SOA), which is shown in Fig. 10, was defined based on the failure distributions. Finally, 120 MOSFETs from the production distribution were subjected to one of two specific UIS stresses along the defined SOA, one group at 30A for 4µs and one group at 5A for 50µs, with each sample getting 100 individual pulses at the stress condition of interest, allowing sufficient time for cooling between pulses. Finally, these 120 parts were distributed into either high temperature gate bias (HTGB, at V_{GS} = 15V at 150°C) or accelerated high temperature reverse bias (HTRB, at V_{DS} >1150V at 150°C) reliability tests to examine if the UIS stress pulses imparted any latent damage into the MOSFETs. The HTRB was performed at an accelerated condition in an attempt to pull out small fractions of the population that might have latent damage, but no parts failed (in the accelerated HTRB or HTGB) in 1000 hours, demonstrating the excellent ruggedness that these MOSFETs have against single-pulse UIS events.

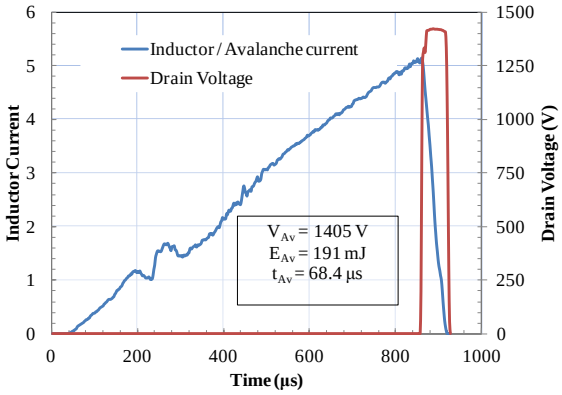

Fig. 9. Unclamped Inductive Switching Waveforms for a 65mΩ/900V Gen 3 SiC MOSFET.

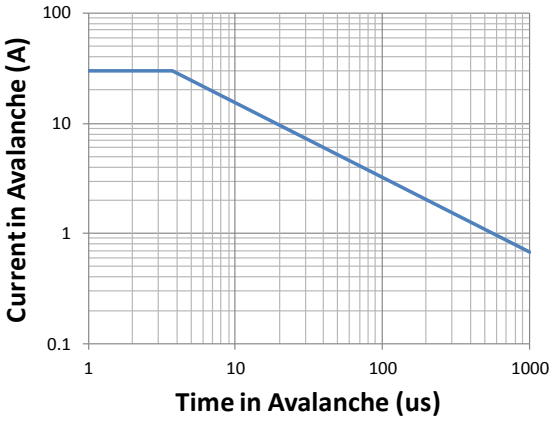

Fig. 10. Unclamped Inductive Switching Safe Operating Area for 65mΩ/900V Gen 3 SiC MOSFETs

SUMMARY

SiC technology is progressing rapidly on several fronts. The SiC material quality has been significantly improved, and concurrently, the wafer diameter is being increased. 150 mm diameter substrates are now widely available, as well as epitaxy on those substrates. These are showing negligible mircopipe densities, and the overall defect densities have been reduced significantly. The next step up in wafer size will be 200 mm diameter wafers and epitaxy, which will allow further reductions in device cost.

The device technology continues to progress as well. We are fabricating Gen 3 SiC planar MOSFETs that are significantly reduced in specific on-resistance and die size. The reduction in die size allows more die per wafer and higher device yields resulting in cost reduction. At the same time, the ruggedness of these devices has reached a very high level, with Gen 3 MOSFETs demonstrated extremely good avalanche ruggedness that is as good or better than found for silicon power devices.

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