Leveraging Power Electronics Acumen to Accelerate the Adoption Ramp of Gallium Nitride

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Abstract

Despite literature showing the device advantages that GaN-on-Silicon brings versus traditional silicon MOSFET technology, the adoption rate of Gallium Nitride will still take time to ramp in many end equipments including but not limited to power electronics. Accelerating adoption will require reducing traditional barriers common to many new technologies: overcoming new design challenges, system cost, and device reliability. Several concepts will be introduced showing how GaN adoption barriers can be mitigated through leveraging testing and lessons learned from both silicon development and the power electronics industry for these three common new technology barriers.

INTRODUCTION

Power Electronics is an emerging market that looks to benefit from the properties of GaN-on-Silicon (GaN) by leveraging improvements in device properties to increase system-level power density. Power density is a critical figure-of-merit in switch-mode power supplies (SMPS) that is a measure of the total power delivered to the load per unit volume. Improving power density is an important trend in multiple end applications where volume is at a premium or reduction in power supply area can be reallocated to increase board area for processors to increase computing density.

The superior device properties of GaN allow faster switching frequencies and slew rates in SMPS applications that have the indirect effect of shrinking inductors, capacitors, magnetics, and other passive components that often take up the majority of volume in a power supply without compromising its ability to deliver power.

Figure 1 introduces two different device structures and their respective properties for FET technologies that can be applied to SMPS applications. The FET parameters listed are the figures-of-merit that determine the power dissipation in SMPS use applications. FET power dissipation is a limiting factor in designing power supplies for high power density, and by using GaN devices with superior properties, FET power dissipation can be minimized. While Figure 1 provides compelling Figures of Merit values for GaN devices, it does not provide understanding of what it takes to achieve the associated benefits in an actual power supply. Examining examples of the application of GaN in power supply scenarios will highlight the enablers for achieving GaN's promise.

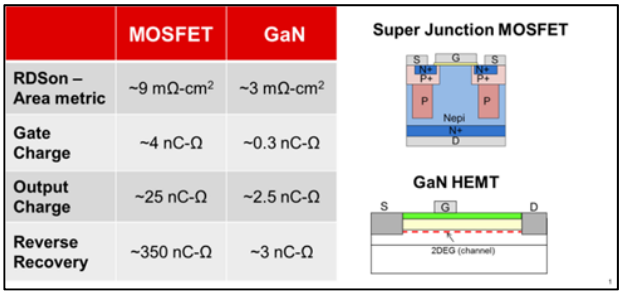


Fig. 1. FET technology cross sections and comparative device figures-of-merit. [1] [2]

Different applications will take advantage of lower power dissipation to enable non-traditional architectures. Figure 2 shows a practical example of a datacenter power distribution system and how GaN increases power density through two architecture changes. The first change is from a traditional Dual Boost architecture to a Totem Pole architecture. The following example shows how this architecture takes advantage of GaN's lack of reverse recovery charge (Qrr) to reduce volumes by as much 30%. The second architecture change is moving from a traditional two-stage bus converter architecture to a single-stage, 48V-to-PoL converter. This architecture can deliver 4x power density improvements by eliminating an entire DC/DC stage.

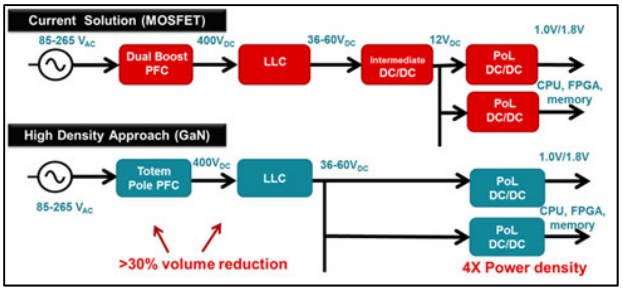


Fig. 2. Powering the next-generation data center with GaN.

POWER SUPPLY DESIGN CHALLENGES

The ecosystem of a SMPS goes beyond that of just the semiconductor power devices. Common components include magnetic transformers for galvanic isolation, analog or digital pulse-width modulated controllers for voltage regulation, and gate drivers to control turning on and off the power devices. Traditional ecosystem components have been optimized for many years around the performance of silicon power devices. However, at an application level these existing ecosystem components either may not function properly with GaN or not enable the full performance.

SMPS design variables can commonly be characterized in one of the three following areas:

1. System architecture selection – GaN enables non-traditional SMPS power supply topologies that are unachievable with silicon
2. Circuit design optimization – GaN operates at slew rates several times higher than silicon, thus requiring higher attention to circuit parasitic elements and layout
3. Component selection availability – GaN forces additional requirements on the surrounding system components especially as higher switching frequencies makes magnetic design and timing control more complicated

One emerging system architecture with GaN is the hard-switched, continuous conduction mode Totem Pole topology targeted for the power factor correction (PFC) stage in an AC/DC power supply. We have found this topology takes full advantages of GaN's lack of reverse recovery charge and lower capacitances to increase switching frequency by 200% while reducing power dissipation by 15%. The end result is an increase in power stage power density by 50% vs. traditional topology implementations.

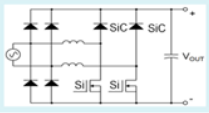
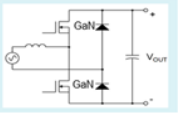
	Figure-of-Merit	Si Dual-Boost	GaN Totem-Pole
Topology			
System Performance	Power Density	60 W/in³	>125 W/in³
	Efficiency	98.7%	99.0%
	Switching Frequency	50 kHz	150 kHz
Power Losses	FET + Diode Conduction	6.6 W	4.4 W
	FET + Diode Switching	2.3 W	2.5 W
	Rectifiers & Inductors	4.5 W	4.5 W
	Total Losses	13.4 W	11.4 W

Fig. 3. Optimized topology selection demonstrates system improvements in both power density and efficiency.

One method for circuit design optimization with GaN is to minimize critical loop inductances through higher levels of integration and novel device partitioning to maximize FET timing and control to achieve switching frequencies and transitions several times higher than traditional implementations.

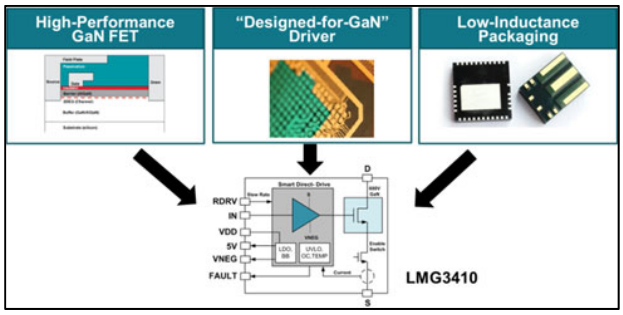


Fig. 4. Example of minimizing circuit inductances through integration of GaN FET, driver, and package with LMG3410.

One specific area of optimization is minimizing the parasitic loop inductances of gate-drive and power loops to ensure intended circuit operation. Parasitic inductances are the result of non-negligible physical dimensions and can be modeled as circuit elements. Developing SMPS with GaN require additional focus on mitigating the effects of parasitic elements to avoid problems such as over voltage stress and shoot-through. Innovative partitioning can minimize loop inductances through a combination of driver integration and low-inductance packaging. Figure 4 shows an innovative partitioning and integration strategy to minimize these parasitic elements.

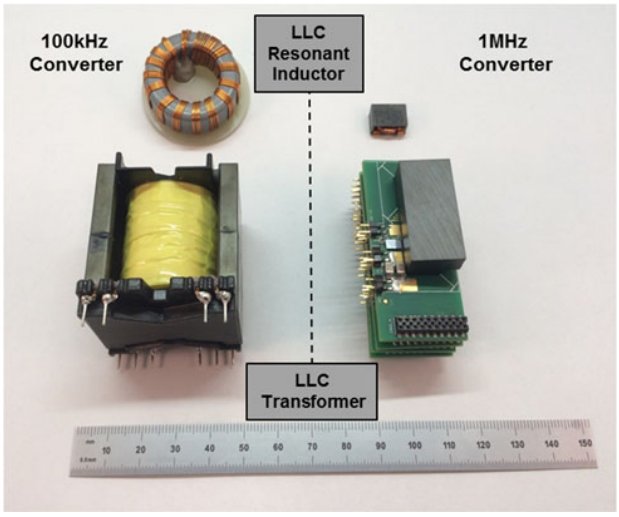


Fig. 5. Example of magnetic volume reduction by increasing frequency from 100kHz to 1MHz.

Component selection for passive components such as inductors, capacitors, and transformers requires additional attention due to requirements to perform at higher switching

frequencies. Figure 5 shows a comparison between two transformers each intended for a 1000W SMPS application in a common power topology known as the LLC with similar power dissipation. This example shows how planar magnetics can achieve smaller form factors.

System Cost Benefits

Consistent manufacturing improvements have historically driven down semiconductor device prices setting an inherent expectation for new technology to be cost competitive. While device cost may be the most intuitive method to compare different semiconductor technologies directly, it may not be the most representative of the criteria power supply designers will use to determine adoption. Figure 6 shows how using GaN in an optimized architecture reduces the total power supply cost.

There are three significant sets of components that drive cost in a power supply:

1. Semiconductor devices such as diodes, FETs, control ICs, and FET drivers
2. Passive components such as capacitors, inductors, transformers, and heat sinks
3. EMI and safety devices such as filter chokes, capacitors, and magnetics

GaN reduces system cost by lowering the total cost of passive components more than the total cost addition from semiconductor devices. The previous example in Figure 3 shows how GaN enables faster switching frequencies and higher power supply efficiency. Increasing from 50kHz to 150kHz enables the use of smaller, lower cost passive components. Increasing from an efficiency of 98.7% to over 99.0% enables smaller mechanical heatsinks or reduces the dependency on forced air cooling. The resulting system cost analysis shows a total reduction of 4% with a 30% reduction in passive components offsetting a 10% increase in semiconductor content.

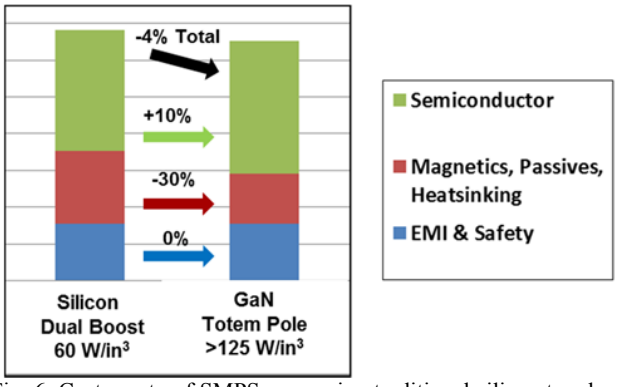


Fig. 6. Cost pareto of SMPS comparing traditional silicon topology vs. emerging topology enabled by GaN.

GaN Reliability Methodology

Reliability for new technology must always be assessed and quantified. New technologies have different failure modes, which require the development of new reliability methodologies. Furthermore, technology uses evolve with time as new capabilities become available and markets develop. Present qualification standards are based on methodologies developed over twenty years ago and will continue to evolve [3], since standards lag technology introduction. For example, the use of power transistors in switching applications has significantly increased over this time. A key part of adoption-ramping is the assurance of technology reliability under actual-use conditions.

One does not need to wait for standards in order to make technology reliable. In order to qualify GaN, we are supplementing present silicon standards-based testing with a knowledge-based approach of GaN technology and its use conditions. This needs not only a deep knowledge of GaN and its failure modes but also the acumen of power electronics usage. It allows us to craft a complete approach to assure that technology is reliable for actual-use conditions.

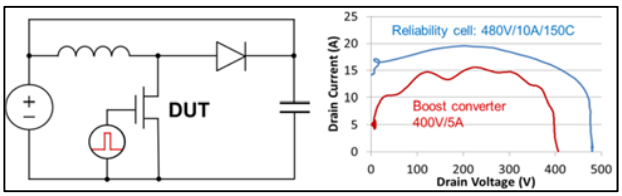


Fig. 7. Double-pulse test circuit and corresponding voltage-current switching locus.

In particular, typical silicon qualification [3] does not address the switching conditions of power management. JEDEC documentation, however, provides guidance on the topic, e.g. [4]. We have thereby identified hard-switching as an application stress condition common to the class of power management devices and are using a simple test vehicle (Figure 7) to apply the stress [5]. This approach reduces the problem to one of a device and a tester. Our test vehicle is the well-known double-pulse tester and it is able to provide accelerated hard-switching stress as shown in Figure 7. By use of the hard-switching test vehicle, we can also measure two key failure modes. The first, dynamic Rds-on degradation, is specific to GaN and occurs due to charge trapping [5].

The second is that of device robustness to switching, which needs to be demonstrated for all technologies. We show that devices that pass both standard qualification testing *and* hard-switching testing run robustly in application. This is illustrated in Figure 8, which shows the stable running of sixteen half-bridge EVM cards for over a

year. In contrast, devices that show dynamic Rds-on degradation with hard-switching get more lossy and overheat with system-level usage [6]. In the case of the LMG3410 product, the built-in over temperature detection circuitry stops the devices before thermal damage occurs.

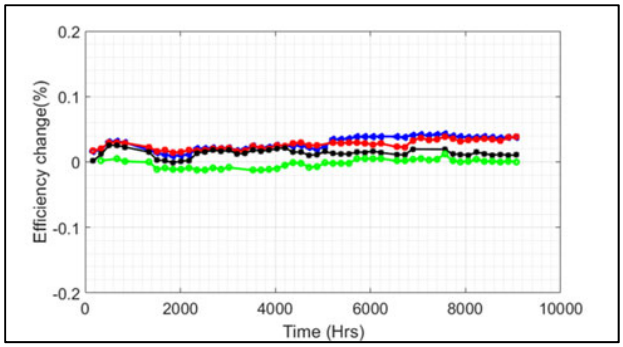


Fig. 8. Demonstration of stable GaN device operation in application-based environment.

CONCLUSIONS

GaN has superior device characteristics that can superior power densities over twice that of traditional silicon-based SMPS designs. The previous examples demonstrate how this performance can be realized by overcoming several traditional new technology barriers including system design challenges, device reliability, and solution cost

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ACRONYMS

GaN: Gallium Nitride
SMPS: Switch-mode Power Supply
MOSFET: Metal-Oxide Field-Effect Transistor
Qrr: Reverse Recovery Charge
PFC: Power Factor Correction