Study of Current Collapse in Single (AlGaN/GaN) and Double (AlGaN/GaN/AlGaN) Heterostructure Enhancement Mode HEMTs

Chun-Hsun Lee[1], Shin-Yi Ho[1], Jin-Xiang Zhang[2], Huang-Kai Lin[2], Jian-Jang Huang[1,*]

[1]Graduate Institute of Photonics and Optoelectronics, National Taiwan University, Taipei 106, Taiwan
[2]Neoton Optoelectronics, Inc., Taiwan
e-mail: r04941101@ntu.edu.tw, *jjhuang@ntu.edu.tw**, Phone: 886-2-3366-3665, FAX: 886-2-2367-7467

Keywords: GaN, enhancement mode, high-electron mobility transistor, current collapse

Abstract

Current collapse is a phenomenon which increase dynamic Ron when the device is operated in high gate and drain bias stress condition. In this research, Al2O3/p-GaN/AlGaN/GaN Enhancement-mode (E-mode) MIS-HEMTs are fabricated. The phenomena of current collapse are discussed between the single heterostructure (SH) MIS-HEMT and double heterostructure (DH) MIS-HEMT. Unlike general researches that focus on the surface modulation to eliminate the phenomenon, this research provides another solution from the perspective of redesign of the material structure. With an AlGaN bottom barrier, the electron confinement of DH remains strong and stable. The better backside confinement suppresses the 2DEG spillover into buffer layer. Thus, the effect of current collapse can be reduced.

Introduction

Wide bandgap gallium nitride (GaN) high-electron mobility transistors (HEMTs) have been regarded as fantastic candidates for power devices. Due to its wide bandgap, GaN power devices feature on high breakdown voltage and good thermal stability. Moreover, the switch frequency of GaN power devices can be very high because of its 2DEG channel with high electron mobility. Hence, these superior physical and material properties making it an excellent candidate for power electronics with performance overwhelm the silicon-based power devices.

The major obstacle that limits the performance and reliability of AlGaN/GaN HEMTs for power switching is the phenomenon of current collapse. The current collapse is caused by the material defects in the transistor structure. Electrons are trapped on the device surface under a negative gate bias, which cannot respond to the sudden change of gate voltage, leading to the depletion of part of the channel carrier and decrease the output current.

In this work, current collapse was investigated in the MIS structure p-GaN/AlGaN/GaN E-mode HEMT structure with double heterostructure.

Device Fabrication

Device fabrication process was carried out on an epitaxial structure consisting of a carbon-doped buffer layer, a GaN layer, a $Al_{0.25}Ga_{0.75}N$ layer and a 60 nm Mg^{+} doped p-GaN layer grown on a Si substrate with the (111) plane by metal organic chemical vapor deposition (MOCVD). The process began with mesa isolation using inductively coupled plasma reactive ion etching (ICP-RIE) in order to reduce leakage current. Next, the p-GaN layer was etched except the gate contact island. There was roughly 5nm residual p-GaN left on the etched area. The source/drain ohmic contact formation was formed by electron beam evaporation of Ti/Al/Ni/Au multilayers and lift-off, followed by rapid thermal annealing at 900°C for 30s in N_2 ambient. The high-k gate insulator was implemented with 10-nm Al_2O_3 grown by Atomic Layer Deposition (ALD). The gate Schottky contact was implemented with Ni/Au evaporation and lift-off. The detailed process flow can be referred from our previous works [1-2]. In this paper, two types of p-GaN HEMTs were under testing. The single heterostructure (SH) device is defined as device A while device B is the transistor with double heterostructure (DH).

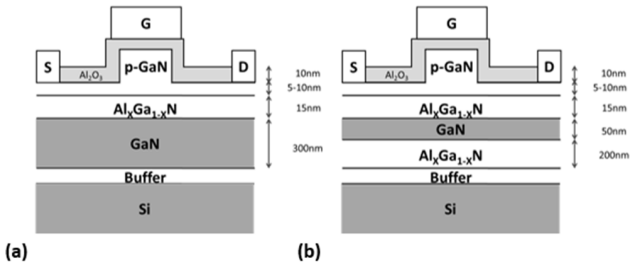

Fig. 1. Epi-Structure of (a) device A and (b) device B.

Results and Discussion

The transfer characteristics of the devices are shown in Fig. 2, along with the output characteristics are shown in Fig.3. The threshold voltage of device A and device B extracted from the linear extrapolation of the transfer characteristics is 0.52V and 1.49 V, respectively, demonstrating an E-mode operation of our devices.

In comparison, device A and device B exhibits an operating current of 148.6 mA/mm and 62.5 mA/mm at gate-source voltage, V_{GS}, of 5 V and V_{DS} of 5 V, respectively. At the same bias condition, the drain current of DH MIS-HEMT is smaller because the total carrier number in 2DEG is smaller, as compared with SH MIS-HEMT [6,7].

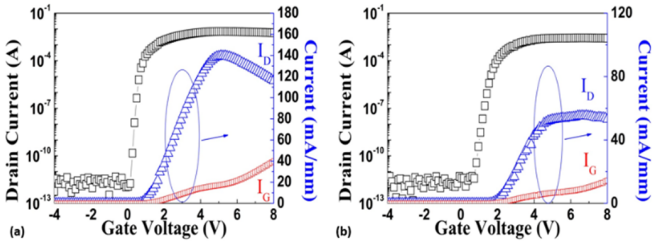

Fig. 2. Transfer characteristics of (a) device A and (b) device B. The drain current is shown in logarithmic (left axis) and linear (right axis) scales.

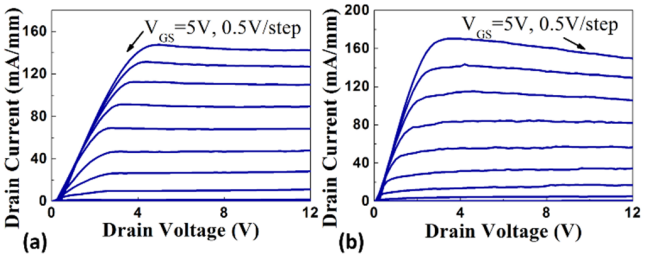

Fig. 3. Output characteristics of (a) device A and (b) device B.

The current collapse measurement setup is shown in Fig. 4(a). The load resistor, R_{LOAD}, is adjusted so that the channel resistance is reasonably measured in the linear region at the on-state. A pulse generator supplies a pulse signal to the gate. Agilent 4155C and its expander unit 41501B were used to provide V_{DS} and V_{GS} simultaneously. We recorded the waveforms from node V_G and V_D with an oscilloscope, LeCroy WaveRunner 6050A. The transient response of the device switched on and off is illustrated in Fig. 4(b). The variation in Ron was evaluated by switching the devices from off-state to on–state by means of short voltage pulses with the period of 25µs and 20% duty cycle. Since our devices are E-mode operation, the measurement voltage of V_G in Fig. 4(b) is 4V while the gate bias stress ranges from 0 to -15V at a step of 5V. Considering the capacitance effect in the real case, V_D will behave as the red line illustrated in Fig. 4(b) instead of the dashed line in Fig. 4(b).

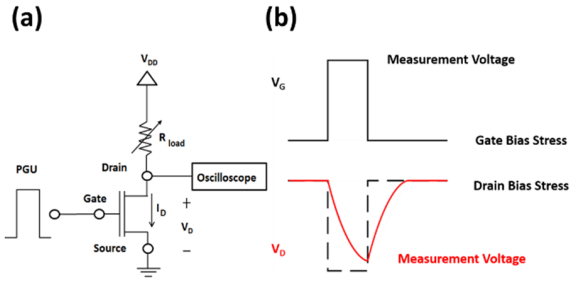

Fig. 4. (a) Illustration of the setup for current collapse measurement; (b) The waveform of the node V_G and V_D in the dynamic measurement. V_{DD} is 40V in the test.

The effect of current collapse under a short pulse stress is examined. At a low V_{DD} level (V_{DD} = 10V), transient responses of the devices are shown in Fig. 5(a) and (b). With the increase of gate bias stress, V_{DS} becomes higher due to as lower drain current, which indicates the phenomenon of current collapse. The effect is less obvious for DH-MIS HEMT than that for SH MIS-HEMT.

Furthermore, the drain current of SH MIS-HEMT can't recover from degradation before post gate bias stress, while the influence of current collapse is less severe for DH MIS-HEMT structure. Current collapse phenomena in the DH MIS-HEMT are suppressed in short pulse mode, as compared with the case in the SH MIS-HEMT.

To understand the mechanism of suppressed current collapse in DH MIS-HEMT, the band diagrams of the HEMT structures are schematically drawn in Fig. 6(a) and Fig. 6(b). DH structure has better carrier confinement in the delta-shaped quantum well, which limits electrons spillover toward the GaN bulk. The 2DEG distribution width in DH is thus narrower than that in SH, but with a higher peak electron density. Furthermore, it is more difficult to deplete 2DEG carriers with a higher peak density and a narrower distribution in the delta-shaped quantum well, thus maintaining carrier stability in the channel for DH structure.

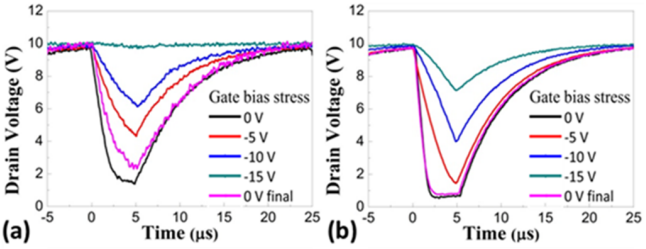

Fig. 5. Transient responses of drain voltage with the pulse period of 5µs. (a) SH MIS-HEMT with V_{DD} = 10V; (b) DH MIS-HEMT with V_{DD} = 10V. The gate bias stress is 0, -5, -10 and -15V, and the post stress measurement is called "0V final".

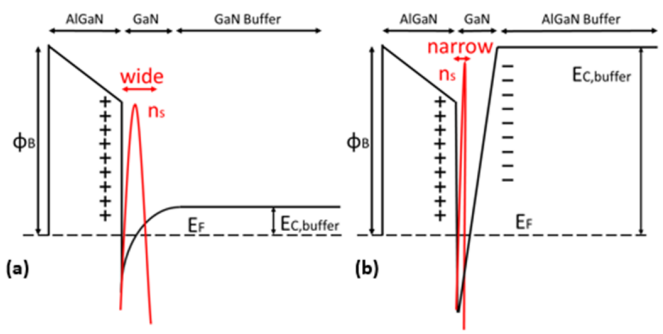

Fig. 6. Band diagram of (a) SH MIS-HEMT and (b) DH MIS-HEMT. The 2DEG distribution width in (b) is narrower than that in (a).

CONCLUSION

In this work, an AlGaN/GaN/AlGaN double heterostructure was proposed for enhancement mode operations. Compared to SH MIS-HEMT, the DH MIS-HEMT shows a higher threshold voltage and lower drain current under the same bias condition. The current collapse measurement shows superior properties of DH MIS-HEMT in pulse measurement. The suppression of current collapse is mainly attributed to the raise of conduction band in the 2DEG channel, resulting in better electron confinement but less total electron density. The results indicate the potential of power applications of the p-GaN/AlGaN/GaN/AlGaN E-mode HEMT structure.

REFERENCES

[1] L.-Y. Su, F. Lee, and J. J. Huang, "Enhancement-Mode GaN-Based High-Electron Mobility Transistors on the Si Substrate With a P-Type GaN Cap Layer," Electron Devices, IEEE Transactions on, vol. 61, pp. 460-465, 2014.

[2] F. Lee, L.-Y. Su, C.-H. Wang, Y.-R. Wu, and J. J. Huang, "Impact of Gate Metal on the Performance of p-GaN/AlGaN/GaN High Electron Mobility Transistors," Electron Device Letters, IEEE, vol. 36, pp. 232-234, 2015.

[3] M. Hatano, Y. Taniguchi, S. Kodama, H. Tokuda, and M. Kuzuhara, "Reduced gate leakage and high thermal stability of AlGaN/GaN MIS-HEMTs using ZrO2/Al2O3 gate dielectric stack," Applied Physics Express, vol. 7, p. 044101, 2014.

[4] Z. Tang, Q. Jiang, Y. Lu, S. Huang, S. Yang, X. Tang, and K. J. Chen, "600-V Normally Off/AlGaN/GaN MIS-HEMT With Large Gate Swing and Low Current Collapse," IEEE Electron Device Letters, vol. 34, pp. 1373-1375, 2013.

[5] S. Arulkumaran, L. Z. Hong, N. G. Ing, S. L. Selvaraj, and T. Egawa, "Influence of Ammonia in the Deposition Process of SiN on the Performance of SiN/AlGaN/GaN Metal-Insulator-Semiconductor High-Electron-Mobility Transistors on 4-in. Si (111)," Applied Physics Express, vol. 2, p. 031001, 2009.

[6] M. Anand, G. Ng, S. Vicknesh, S. Arulkumaran, and K. Ranjan, "Reduction of current collapse in AlGaN/GaN MISHEMT with bilayer SiN/Al2O3 dielectric gate stack," physica status solidi (c), vol. 10, pp. 1421-1425, 2013.

[7] I. Hwang, J. Kim, S. Chong, H.-S. Choi, S.-K. Hwang, J. Oh, J. K. Shin, and U.-I. Chung, "Impact of channel hot electrons on current collapse in AlGaN/GaN HEMTs," IEEE Electron Device Letters, vol. 34, pp. 1494-1496, 2013.

ACRONYMS

HEMT: High electron mobility transistor
E-mode: Enhancement mode
DH: Double heterostructure
SH: Single heterostructure
Vth: Threshold voltage
ICP-RIE: Inductively coupled plasma reactive ion etching