Optimized Design of 3-Dimensional Field Plate in AlGaN/GaN HEMTs for Collapse-Free Operation

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Abstract

We have fabricated an AlGaN/GaN HEMT with a 3-dimensional field plate (3DFP), in which a multi-grooved and fin-shaped gate field plate (G-FP) was successfully introduced. By the optimization of groove parameters, such as groove depth and groove spacing, we were able to maximize the mitigation effect in current collapse by 3DFP and achieved almost current collapse-free operation up to a drain voltage of 150 V.

INTRODUCTION

GaN is featured as a wide-bandgap, high breakdown field, and high electron mobility material. It is thus widely recognized that an AlGaN/GaN HEMT is promising as a next-generation power device with capabilities for low-loss and high-voltage switching applications [1,2]. However, the degradation in dynamic on-resistance due to current collapse still remains as a serious problem in AlGaN/GaN HEMTs. This is believed to be due to trapping effects observed during on/off power switching operation [3].

Use of a field plate (FP) is well-known as an efficient way to reduce current collapse in GaN-based HEMTs [4]. To maximize its collapse-suppression effect, we have developed a novel 3-dimensional field plate (3DFP) structure, in which a gate field plate (G-FP) is located on fin-like multiple grooves formed in the AlGaN barrier layer [5,6]. In this work, we have studied the effect of groove depth and optimized the groove parameters in 3DFP to achieve further reduction in current collapse.

DEVICE STRUCTURE AND PROCESS

Fig. 1 shows the schematic cross-section of our device structure. We employed a standard AlGaN/GaN heterostructure grown by MOCVD on a SiC substrate. The AlGaN barrier layer is of 25 nm thickness with an Al content of 20%. HEMTs were fabricated with a gate length (L_g) of 3 µm and a gate width (W_g) of 100 µm. The gate-to-drain distance was nominally 10 µm. Devices were passivated with a 100 nm-thick SiN film, on which 3DFP was formed. Figs. 2 (a) and (b) show the plan view and the cross-sectional view of the devices with 3DFP. The FP length, the

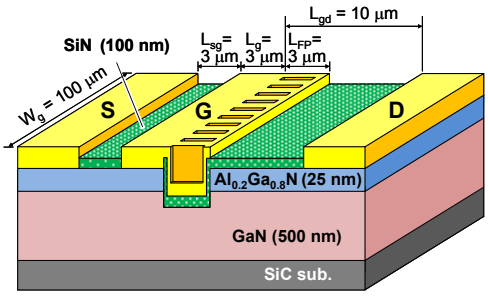

Fig. 1. Cross-sectional view of 3DFP HEMT.

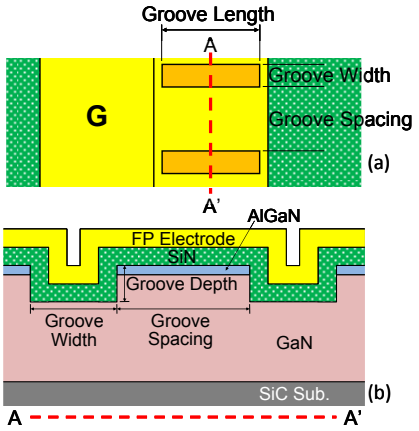

Fig. 2. Plan and cross-sectional views of 3DFP HEMT.

groove length, and the groove width were fixed at 3 µm, 2.5 µm, and 0.3 µm, respectively, while the groove depth and the groove spacing were varied.

The device process started with mesa-isolation using ICP reactive ion etching (RIE) by BCl_3/Cl_2 mixed gases. Source/drain ohmic metallization was made by evaporating Ti/Al/Mo/Au (15/60/35/50 nm), followed by annealing at 850 ºC for 30 s. Then, Ni/Au (50/150 nm) was deposited as a gate electrode. Patterns for fin-like multiple grooves were then made using electron-beam lithography, followed by groove etching using ICP-RIE. After groove formation, 100 nm-thick SiN was sputter-deposited on the whole wafer and then Ti/Au (5/200 nm) was deposited to form 3DFP. The completed device picture and its magnified SEM image are shown in Fig. 3.

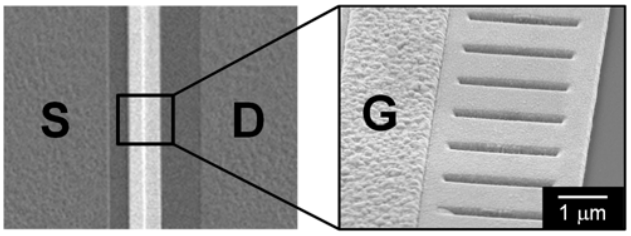

Fig. 3. Picture of 3DFP HEMT and SEM image of 3DFP.

CURRENT COLLAPSE MEASUREMENT

The dynamic on-resistance of the device was measured using the circuit shown in Fig. 4. The load resistance (R_L) was adjusted so that the measured on-current was within the linear region. The on-state and off-state duration times for the gate pulse were 10 μs and 10 ms, respectively. As a measure of current collapse, the normalized dynamic on-resistance (NDR) was defined by the measured dynamic on-resistance divided by the value of static on-resistance. Note that NDR=1 means collapse-free operation.

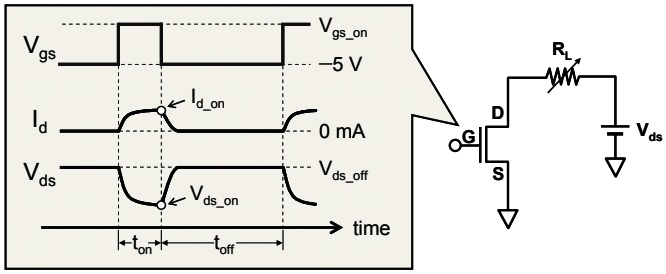

Fig. 4. Current collapse measurement circuit.

RESULTS AND DISCUSSION

Since grooves for 3DFP were formed by ICP-RIE in the active channel region, there is a concern that device characteristics may be degraded by plasma damage. To investigate how the plasma damage affects device performance, we measured DC characteristics of 3DFP HEMTs with various groove spacings, while the groove width was fixed at 0.3 μm. TABLE I lists typical DC characteristics of the conventional HEMT without FP (device A), conventional HEMT with G-FP (device B), and 3DFP HEMTs with a groove spacing from 0.3 to 0.9 μm. Compared to devices A and B (without 3DFP), it is evident that 3DFP HEMTs with a narrower groove spacing show significant degradation in both maximum drain current (I_{dmax}) and on-resistance (R_{on}). However, a 3DFP device with a groove spacing of 0.9 μm exhibited almost negligible degradation in I_{dmax} with only a slight increase in R_{on} by less than 20 %. Fig. 5 compares DC characteristics of device B and the 3DFP device with a groove spacing of 0.9 μm. Both DC characteristics show essentially the same characteristics.

TABLE I SUMMARY OF DC CHARACTERISTICS.

	w/o FP Device A	With FP Device B	3DFP, Groove Spacing			
			0.9 μm	0.6 μm	0.45 μm	0.3 μm
I_{dmax} (A/mm) @V_g= 1 V	0.36	0.36	0.36	0.24	0.19	0.09
R_{on} (Ωmm)	14.3	14.5	17.3	19.1	23.6	37.4

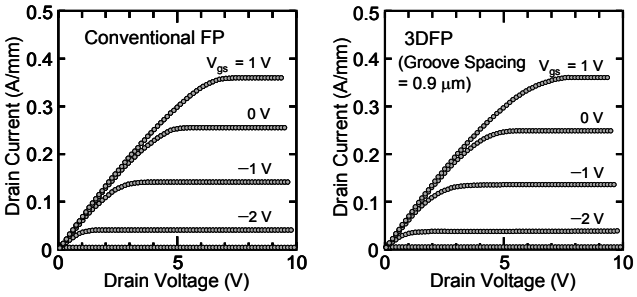

Fig. 5. Drain I-V characteristics.

Fig. 6 shows the dependence of normalized dynamic on-resistance (NDR) on the off-state drain stress voltage. In the measurements, the gate voltage was switched from -5 V during off-state to +1 V during on-state. The NDR for device A (w/o FP) was found to increase significantly to about 500 with increasing the off-state drain voltage (V_{ds}) from 20 to 150 V. It is evident that NDR for device B (conventional G-FP) was reduced by an order of magnitude as compared to device A. Nevertheless, device B exhibited gradual degradation in NDR with increasing V_{ds}. Such residual degradation in NDR can be almost completely suppressed by introducing 3DFP, resulting in an NDR value of less than 1.1 even at V_{ds}=150 V.

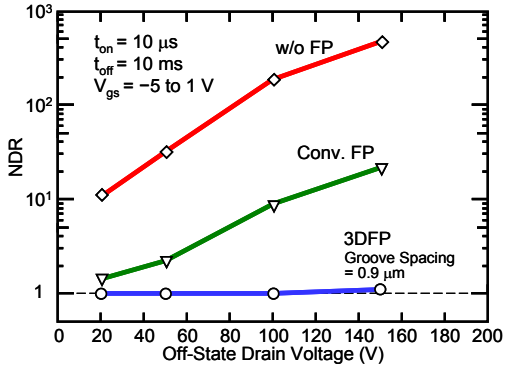

Fig. 6. NDR as a function of off-state drain voltage.

Fig. 7 shows the measured NDR as a function of the on-state gate voltage (V_{gs}). The NDR for FP devices (device B and 3DFP devices) was improved as V_{gs} was increased from -1 to +1 V, while no such behavior was observed for device A (w/o FP), in which NDR was kept constant at around 500 over the whole V_{gs} range investigated. It should be noted that the 3DFP device with a groove spacing of 0.9 μm exhibited

almost collapse-free operation when V_{gs} was increased to +1 V.

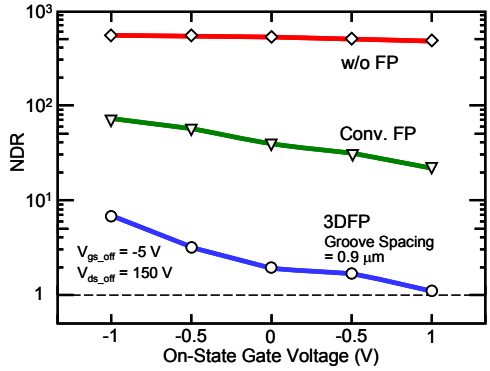

Fig. 7. NDR as a function of on-state gate voltage.

Fig. 8 shows the NDR as a function of the groove depth in 3DFP devices. The NDR was improved as the groove depth was increased, resulting in collapse-free operation (NDR<1.1) for a groove depth of more than 150 nm. Fig. 9 shows the measured static on-resistance as a function of the

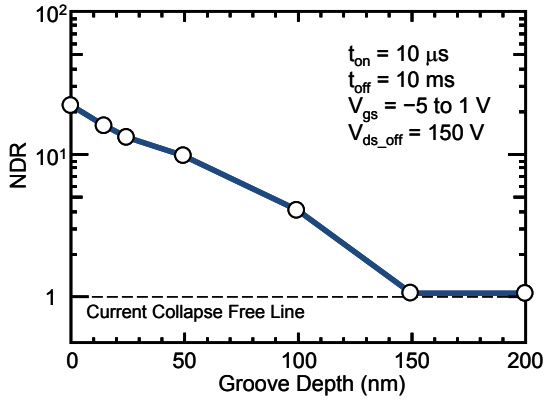

Fig. 8. NDR as a function of groove depth.

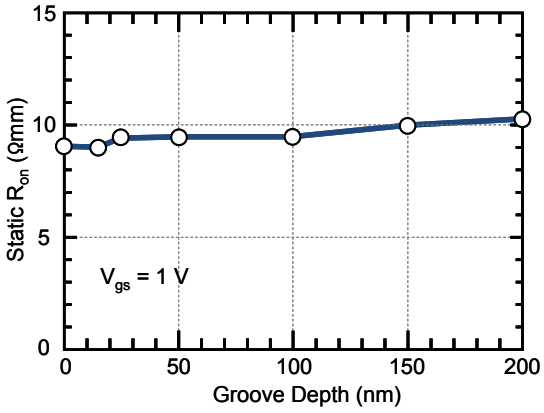

Fig. 9. Static on-resistance as a function of groove depth.

groove depth. With increasing the groove depth, part of 2-dimensional electron Gas (2DEG) under the groove area was depleted, thus leading to an increase in the on-resistance. However, as shown in Fig.9, the degradation in the on-resistance, estimated at V_{gs}=+1 V, was very small, i.e., within 15% even at a groove depth of 200 nm. Correspondingly, the decrease in the maximum drain current was also negligibly small (about 10 %) at 200 nm of groove depth.

Fig. 10 depicts schematically the mechanism why 3DFP is effective to suppress current collapse. The schematic cross-sections of 3DFP for shallow and deep grooves are shown in Figs. 10(a) and (b), respectively. When the groove is rather shallow (15-50 nm), the bottom of the FP electrode is still far away from the 2DEG channel, thus leading to insufficient current collapse reduction. This situation can be modeled by the effective field plate capacitance (C_{FP}), which is not large enough due to rather large separation between FP and 2DEG. However, when the groove depth is increased so that the bottom of FP comes into line with the 2DEG channel, as shown in Fig. 10(b), the reduced separation between FP and 2DEG forms a large C_{FP}, supplying enough incremental electron charge $\Delta Q = C_{FP}\Delta V_{gs}$ into the 2DEG channel during the period of on-state. This is the main reason why 3DFP is superior to conventional FP in suppressing current collapse and finally realizes almost collapse-free operation.

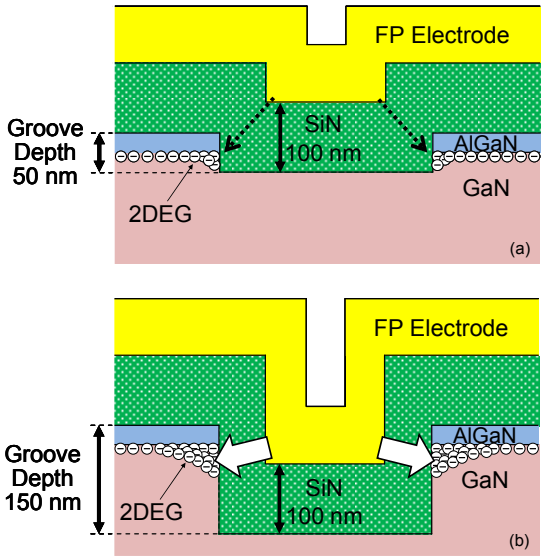

Fig. 10. Models to explain suppressed current collapse by 3DFP. Groove depth of 50 nm (a) and 150 nm (b).

CONCLUSIONS

We have fabricated AlGaN/GaN HEMTs with a 3DFP structure and investigated the effect of groove parameters on the dynamic on-resistance. By optimizing the groove depth and groove spacing of 3DFP, we were able to maximize the current collapse mitigation effect by 3DFP and finally

achieved almost current collapse-free operation up to a drain voltage of 150 V.

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ACRONYMS

HEMT: High Electron Mobility Transistor
FP: Field Plate
NDR: Normalized Dynamic On-Resistance
2DEG: 2-Dimensional Electron Gas