Improved Uniformity on E-mode GaN-on-Si MIS-HEMTs Fabrication by High-Temperature Gate Recess Technique

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Abstract

A high-temperature (180 °C) gate recess technique featuring high uniformity and low damage is developed to improve the etching surface of GaN-based devices. In this work, we carried out a comprehensive study on the effects of the recess on the electrical properties of metal/AlGaN interface. Improved uniformity in Schottky barrier height(SBH) and ideality factor are confirmed. With high-temperature gate recess, Enhancement-mode GaN-on-Si metal-insulator-semiconductor high electron mobility transistors (E-mode MIS-HEMTs) with high threshold voltage (V_{TH}) and high field-effect mobility (μ_{FE}) were fabricated.

INTRODUCTION

Recess etching of AlGaN/GaN heterostructure plays a vital role in the fabrication of high performance GaN-based RF/microwave power amplifiers and also enhancement-mode (E-mode) lateral power devices. Low-damage recessing of the AlGaN barrier will not only enhance the cutoff frequency of GaN-based high-electron-mobility transistors (HEMTs), but also facilitate the fabrication of high threshold voltage (V_{TH}), low ON-resistance E-mode metal-insulator-semiconductor HEMTs (MIS-HEMTs) [1-5]. The latter is regarded as one of most promising technologies for next-generation GaN power device [6-8].

Inductively coupled plasma (ICP) dry etching is an attractive technique to develop E-mode GaN-based devices owing to its anisotropy etching and high efficiency. However, conventional room-temperature (RT) ICP dry etching tends to induce non-negligible physical plasma damage, which consequently leads to high interface trap density and lower channel mobility. To improve the etching surface, a high-temperature (180 °C) gate recess technique featuring high uniformity and low damage is developed [8,9]. High-temperature (HT) gate recess technique can promote in-situ desorption of chlorine-based etching residues and repair the lattice damages, which results improved power and RF performance.

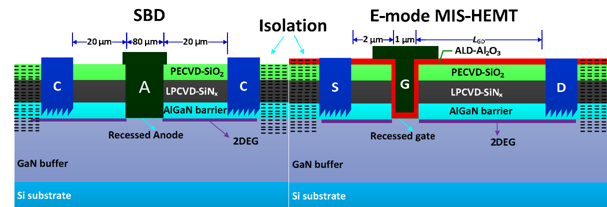

Fig. 1. Schematic cross-sectional views of the AlGaN/GaN anode-recessed SBDs and E-mode MIS-HEMTs on Si substrates. The gate-to-drain distance (L_{GD}) of E-mode MIS-HEMTs ranges from 3 μm to 21 μm.

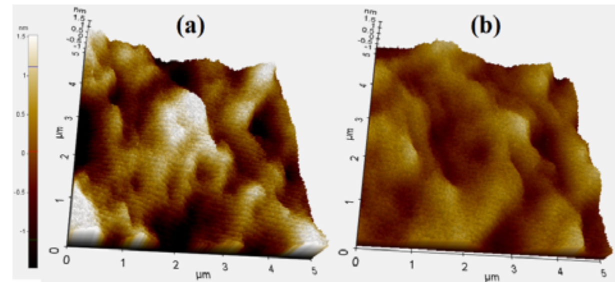

Fig. 2. Atoms force microscope 3-D images of the AlGaN surface after 2-min dry-etching. (a) Recess at room temperature (RT). (b) Recess at 180 °C (HT).

In this work, AlGaN/GaN anode-recessed Schottky barrier diodes (SBDs) and E-mode MIS-HEMTs (shown in Figure 1) are fabricated by using the high-temperature low-damage gate recess technique. We systematically research the uniformity of HT gate recess technique in contrast with RT reference by atoms force microscope in Figure 2. Improved uniformity in Schottky barrier height (SBH) and ideality factor are confirmed. With high-temperature gate recess, Enhancement-mode GaN-on-Si metal-insulator-semiconductor high electron mobility transistors (E-mode MIS-HEMTs) with high V_{TH} and high field-effect mobility (μ_{FE}) were fabricated.

DEVICE FABRICATION

AlGaN/GaN epi-structures in this work were grown on a Si substrate by metal organic chemical vapor deposition and

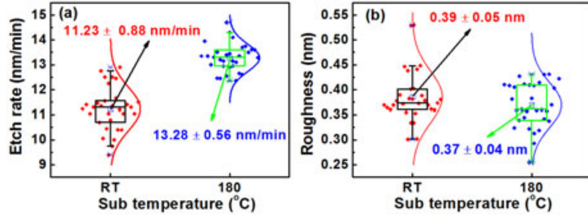

Fig. 3. (a) The etch rate and (b) roughness of RT and HT dry-etching.

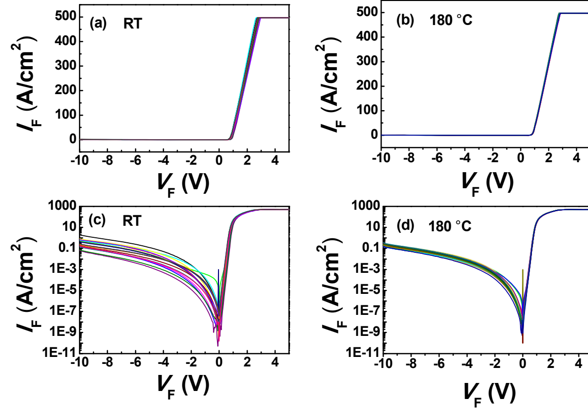

Fig. 4. The measured forward *I-V* curves anode-recessed SBDs. (a) RT, linear scale; (b) HT, linear scale; (c) RT, logarithm scale. (d) HT, logarithm scale.

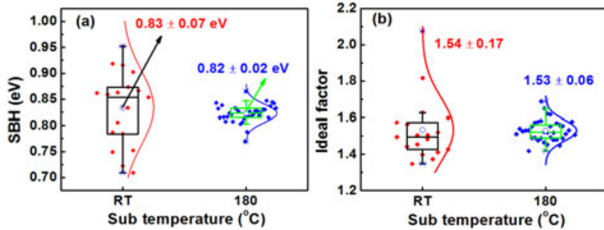

Fig. 5. (a) The Schottky barrier height (SBH) and (b) ideal factor of RT and HT anode-recessed SBDs.

the AlGaN barrier were composed of a 2 nm GaN cap, a 25 nm $Al_{0.22}Ga_{0.78}N$ barrier layer and ~1 nm AlN spacer. The AlGaN/GaN heterostructure features a two-dimensional electron gas (2DEG) sheet resistance of 372 Ω/□ and a channel mobility of 1570 cm^2/V·s. Prior to the device fabrication, we made a series of dry etching experiments to obtain the etch rate and roughness of HT and RT gate recess technique. The process of HT gate recess technique is similar to the process of RT gate recess technique, except that the substrate of wafer was heated up to 180 °C during the ICP dry etch.

Device fabrication for HEMTs/MIS-HEMTs was started with deposition of 100 nm SiN_x layer at 780 °C by low-pressure chemical vapor deposition (LPCVD) as the passivation [10]. The LPCVD-SiN_x in the source/drain contacting area is etched away by ICP dry etching, followed by E-beam evaporation of Ti/Al/Ni/Au metal stack, lift off, and 850 °C annealing in N_2 ambient. Then a 40-nm SiO_2 layer as hard mask for high-temperature gate recess was grown at 300 °C by plasma-enhanced chemical vapor deposition (PECVD) [8]. Device isolation was realized by multiple energy N^+ implantations. Subsequently, the PEVCD-SiO_2 and LPCVD-SiN_x layers in the gate region were removed by fluorine-based plasmas in ICP. After photoresist removal, ICP dry etching with Cl_2/BCl_3 plasma at 180 °C. At the same time, one wafer was processed at room temperature as reference. E-mode MIS-HEMTs were realized by high temperature recess of AlGaN barrier with ~0.5 nm remaining and O_3-assisted atomic-layer-deposition for Al_2O_3 gate dielectric. Both SBDs and MIS-HEMTs were finally carried out the same gate contact formation, with E-beam evaporated Ni/Au bilayer as the gate metal. To improve devices' thermal stability, rapid

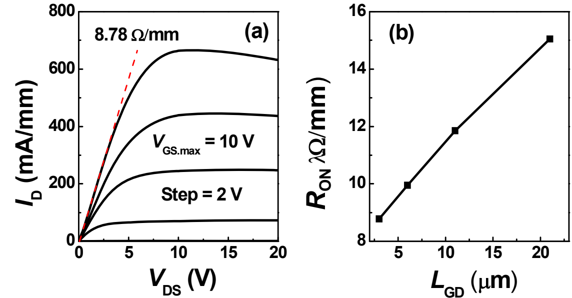

Fig. 6. (a) Output characteristics of the E-mode GaN-based MIS-HEMTs with L_{GD} = 3 μm and (b) the R_{ON} of E-mode MIS-HEMTs with different L_{GD}.

thermal annealing (RTA) at 400 °C for 4 min was performed on both devices.

Results and Discussion

The roughness of the fresh surface of AlGaN surface is 0.26 nm. After 2-min dry etching, the uniformity of etch rate and surface roughness of RT and HT etching measured by atoms force microscope are shown in Figure 2 and Figure 3, respectively. It can be clearly observed that though the HT etch rate is higher (HT 13.28 nm/min, RT 11.23 nm/min), the standard deviation of the HT etch rate is better (HT 0.56 nm/min, RT 0.88 nm/min), indicating an improved etching uniformity by HT recess technique. Moreover, the mean value and the standard deviation of the etched surface roughness of the HT recess technique is 0.37 and 0.04 nm, which is better than RT (mean value is 0.39 nm, standard deviation is 0.05 nm).

Figure 4 shows the typical I-V characteristic of the SBDs from HT and RT techniques, and Figure 5 shows the extracted schottky barrier height and ideality factor. The I-V curve is similar for both techniques, however, the reverse leakage current, schottky barrier height and ideality factor is widely distributed with RT recess technique. It indicates that the HT recess technique features remarkably low surface roughness and high uniformity.

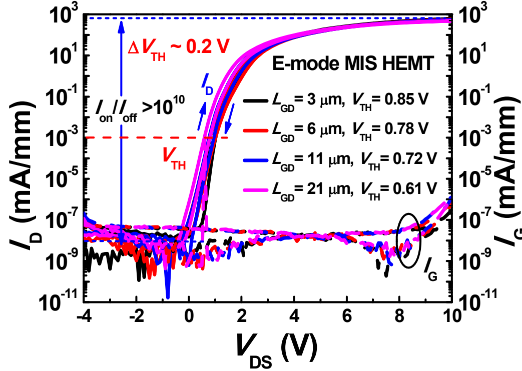

Fig. 7. Transfer characteristics of the E-mode GaN-based MIS-HEMTs with different L_{GD}.

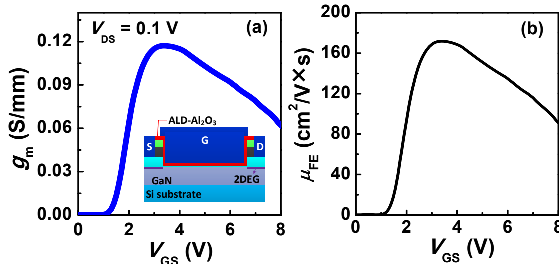

Fig. 8. (a) Transfer characteristic and (b) Experimental field-effect mobility profile of the fat E-mode MIS-HEMTs at V_{DS} = 0.1 V.

E-mode MIS-HEMTs exhibit well-behaved output DC performance (shown in Figure 6) with a maximum drain current density of 665 mA/mm and R_{on} of 8.78 Ω*mm. The transfer I-V curves of the MIS-HEMTs (Figure 7) show state-of-the-art results of uniform V_{TH} (0.85 V ± 0.2V@ 1 μA/mm), a high I_{ON}/I_{OFF} of 10^{10} and low gate leakage (~10^{-8} mA/mm). A high maximum μ_{FE} of 172 $cm^2/V{\cdot}s$ has been achieved in the experimental μ_{FE} profile (shown in Figure 8) determined by high-frequency capacitance-voltage measurements on fat E-mode MIS-HEMTs.The field-effect mobility is extracted using $\mu_{FE} = g_m L_G/(W_G C_{MIS} V_{DS})$ at V_{DS} = 0.1 V, where capacitance of metal-insulator-semiconductor of (C_{MIS}) is 398.2 nF/cm^2. The peak μ_{FE} is lower than the values obtained in the E-mode MIS-HEMTs in Ref. [9], which is 650 $cm^2/V{\cdot}s$ with about 6-nm recessed AlGaN barrier remains. One of the influence factors is the difference in the initial 2DEG mobility of AlGaN/GaN epi-structures. Moreover, the remaining AlGaN barrier thickness plays a critical role in the mobility degradation. Scattering effect of the states at gate-dielectric/recessed-AlGaN interface will increase significantly as the recessed AlGaN barrier is further reduced, or even completely removed.

Conclusions

A high-temperature (180 °C) gate recess technique featuring high uniformity and low damage is developed to improve the etching surface of GaN-based devices. Improved uniformity in Schottky barrier height and ideality factor of metal/recessed-AlGaN interface are confirmed. With high-temperature gate recess, Enhancement-mode GaN-on-Si metal-insulator-semiconductor high electron mobility transistors (E-mode MIS-HEMTs) with high V_{TH} and high field-effect mobility (μ_{FE}) were fabricated. High-temperature recess etching of III-nitrides could be a compelling technique in fabrication of both high-frequency GaN-based power amplifiers as well as high performance E-mode GaN power devices.

Acknowledgements

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References

[1] T. Palacios, A. Chakraborty, S. Rajan, C. Poblenz, S. Keller, S. P. DenBaars, J. S. Speck, and U. K. Mishra, “High-power AlGaN/GaN HEMTs for Ka-band applications,” *IEEE Electron Device Letters*, vol. 26, no. 11, pp. 781-783, Nov. 2005.

[2] W. Saito, Y. Takada, M. Kuraguchi, K. Tsuda, and I. Omura, “Recessed-gate structure approach toward normally off high-Voltage AlGaN/GaN HEMT for power electronics applications,” *IEEE Transaction on Electron Devices*, vol. 53, no. 2, pp.356-362, Feb. 2006.

[3] J. W. Chung, W. E. Hoke, E. M. Chumbes, and T. Palacios, “AlGaN/GaN HEMT With 300-GHz,” *IEEE Electron Device Letters*, vol. 31, no. 3, pp. 195-197, Mar. 2010.

[4] B. Lu, O. I. Saadat, and T. Palacios, “High-Performance Integrated Dual-Gate AlGaN/GaN Enhancement-Mode Transistor,” *IEEE Electron Device Letters*, vol. 31, no. 9, pp.990-992, Sep. 2010.

[5] Z. Xu, J. Wang, Y. Liu, J. Cai, J. Liu, M. Wang, M. Yu, B. Xie, W. Wu, X. Ma, and J. Zhang, “Fabrication of Normally Off AlGaN/GaN MOSFET Using a Self-Terminating Gate Recess Etching Technique,” *IEEE Electron Device Letters*, vol. 34, no. 7, pp. 855-857, Jul. 2013.

[6] M. Kanamura, T. Ohki, T. Kikkawa, K. Imanishi, T. Imada, A. Yamada, and N. Hara, “Enhancement-Mode GaN MIS-HEMTs With n-GaN/i-AlN/n-GaN Triple Cap Layer and High-k Gate Dielectrics,” *IEEE Electron Device Letters*, vol. 31, no. 3, pp. 189–191, Mar. 2010.

[7] [1] Qi Zhou, Bowen Chen, Yang Jin, Sen Huang, Ke Wei, Xinyu Liu, Xu Bao, JinyuMou, and Bo Zhang, “High-

Performance Enhancement-Mode Al2O3/AlGaN/GaN-on-Si MISFETs With 626 MW/cm2 Figure of Merit," *IEEE Transaction on Electron Devices*, vol. 62, no. 3, pp.776-781, Mar. 2015.
[8] S. Huang, Q. Jiang, K. Wei, G. Liu, J. Zhang, X. Wang, Y. Zheng, B. Sun, C. Zhao, H. Liu, Z. Jin, X. Liu, H. Wang, S. Liu, Y. Lu, C. Liu, S. Yang, Z. Tang, J. Zhang, Y. Hao, and K. J. Chen, "High-temperature low-damage gate recess technique and ozone-assisted ALD-grown Al2O3 gate dielectric for high-performance normally-off GaN MIS-HEMTs," *in Proceeding*, *IEEE International Electron Devices Meeting*, pp. 442-445, 2014.
[9] S. Huang, X. Liu, J. Zhang, K. Wei, G. Liu, X. Wang, Y. Zheng, H. Liu, Z. Jin, C. Zhao, C. Liu, S. Liu, S. Yang, J. Zhang, Y. Hao, and K. J. Chen, "High RF Performance Enhancement-Mode Al2O3/AlGaN/GaN MIS-HEMTs Fabricated With High-Temperature Gate-Recess Technique," *IEEE Electron Device Letters*, vol. 36, no. 8, pp. 754–756, Aug. 2015.
[10] X. Wang, S. Huang, Y. Zheng, K. Wei, X. Chen, G. Liu, T. Yuan, W. Luo, L. Pang, H. Jiang, J. Li, C. Zhao, H. Zhang, and X. Liu, "Robust SiNx/AlGaN Interface in GaN HEMTs Passivated by Thick LPCVD-Grown SiNx Layer," *IEEE Electron Device Letters*, vol. 36, no. 7, pp. 666–668, Jul. 2015.

ACRONYMS

E-mode: enhancement-mode
HEMTs: high-electron-mobility transistors
MIS-HEMTs: metal-insulator-semiconductor HEMTs
ICP: Inductively coupled plasma
RT: room-temperature
HT: high-temperature (180 ºC)
SBDs: Schottky barrier diodes
SBH: Schottky barrier height
2DEG: two-dimensional electron gas
LPCVD: low-pressure chemical vapor deposition
PECVD: plasma-enhanced chemical vapor deposition