Pt Gate Sink-In Process Details Impact on InP HEMT DC and RF Performance

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Abstract

The impact of the Pt/Ti/Pt/Au gate sink-in process on the DC and RF performance of AlInAs/GaInAs/InP high electron mobility transistors (HEMTs) is studied with two different approaches for the Pt gate sink–in. Following gate metal deposition, one process split was rapid thermal annealed (RTA) at 250°C and passivated by atomic layer deposition (ALD) at 180°C. For the second split, the Pt gate sink-in was carried out in an ALD system at 250°C simultaneously with the gate passivation. Despite identical sink-in temperatures, the two process splits exhibit different characteristics, implying that not only the temperature but also the sink-in ambient and the thermal ramp rate affect the device manufacturing. To verify this conclusion, one additional sample was subsequently processed with Pt gate sink-in carried out in the RTA at 250°C, with standard process parameters, but without the flow of the forming gas.

Introduction

InP-based High Electron Mobility Transistors (HEMTs) are attractive for high-speed, high-gain and low-noise RF applications both at room and cryogenic temperatures. Their great performance is mainly due to the superior channel transport properties such as high electron mobility and high saturation velocity.

A key parameter determining the performance of InP HEMTs is the transconductance g_M. The value of g_M and short-channel effects sensitively depend on the gate-to-channel separation. Smaller gate-to-channel separations effectively increase g_M and often lead to a rise in the current gain cutoff frequency (f_T), both of which are desirable to achieve good noise performances [1].

Pt buried gate technology can help reduce the gate-to-channel separation because Pt can be controllably diffused into the semiconductor to enable vertical scaling [2]. Gate sink-in technology is thus central to the manufacturing of high-performance HEMTs — we show here that the sink-in ambient and thermal ramp rate for a given temperature affect the reaction of Pt with the underlying semiconductor resulting in a significant impact on device performance.

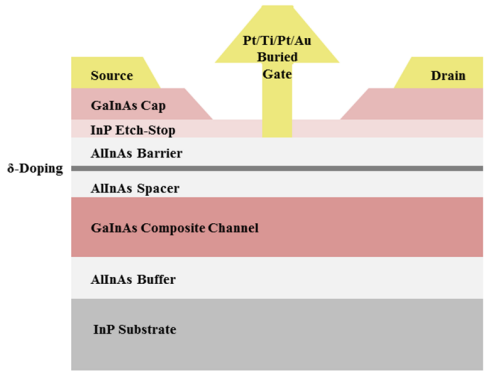

Fig. 1. Schematic cross-section of the fabricated HEMTs.

Device Fabrication

Figure 1 shows a cross-section of our InP-HEMTs [3]. For this study, process splits were implemented based on the same MBE-grown epitaxial layers which feature: semi-insulating InP substrate, AlInAs buffer, GaInAs composite channel, AlInAs spacer, Si δ-doping, AlInAs Schottky barrier layer, InP etch-stop and highly n-doped GaInAs cap layer. Two process splits nominally differed only in the Pt gate sink-in process details.

Device fabrication began with the formation of the source and drain Ohmic contacts by evaporation of Ge/Au/Ni/Au metal stack followed by rapid thermal annealing. Next, the device isolation was performed using wet chemical etching. Following the patterning by electron beam lithography, the gate region was recessed by selective removal of the *n*+ GaInAs cap layer, and the T-gate contact was formed by evaporation and lift-off of a Pt/Ti/Pt/Au metal stack. Following the gate metal deposition, each split was annealed to diffuse Pt through InP etch-stop layer and into the AlInAs Schottky barrier thus reducing the gate-to-channel distance. The first split (A) was annealed in the RTA at 250°C for 10 min in a forming gas (5% H_2 : 95% N_2) ambient with a rapid ramp rate and then passivated with Al_2O_3 by ALD at 180°C. The second split (B) was annealed *during* the Al_2O_3 deposition by ALD at 250°C for 1 hour in vacuum environment with a moderate ramp rate. Both sink-in processes exhibited a low temperature overshoot of less than

2°C. Device fabrication for both splits was completed by an evaporation of a thick Ti/Au overlay metallization.

DEVICE CHARACTERISTICS

Figure 2 shows the DC output and transconductance characteristics measured at 300 K for 2 × 50 μm HEMTs with a gate length of L_G = 50 nm.

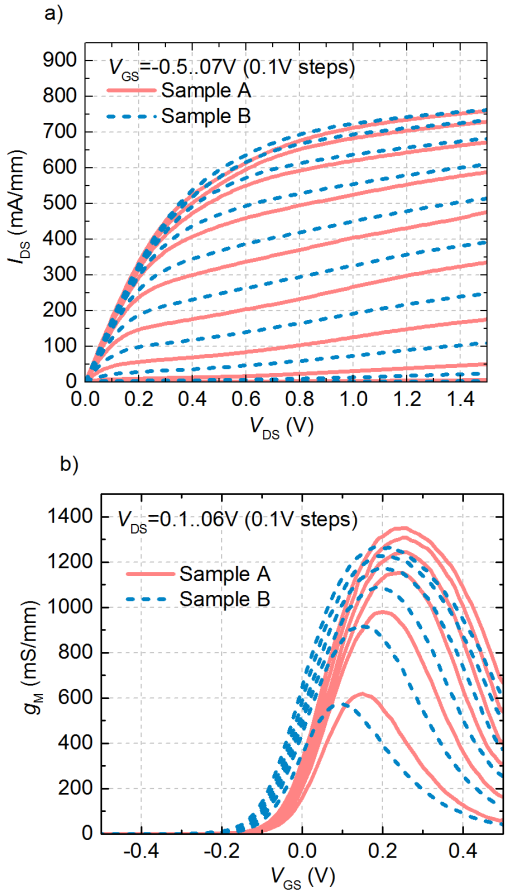

Fig. 2. (a) DC output and (b) transconductance characteristics of fabricated 2 × 50 µm HEMTs with gate length of 50 nm measured at 300 K.

The devices annealed in the RTA (split A) exhibit a more positive threshold voltage V_{th} and a higher DC transconductance g_M with respect those annealed in the ALD (split B) as seen in figure 2. The measured gate leakage current (defined as I_{GS} for V_{DS} = 0 V at V_{GS} = −1 V) is higher for split A, I_{GSA} = 0.8 μA/mm, compared to I_{GSB} = 0.6 μA/mm for split B. These characteristics suggest a smaller gate-to-channel separation when the RTA is used to sink-in the Pt buried gates.

Figure 3 shows the de-embedded f_T obtained from the H_{21} extrapolation as a function of the drain current I_{DS} at V_{DS} of 0.5 V for both splits. Extraction of the small-signal equivalent circuits [4] reveals that the intrinsic small-signal

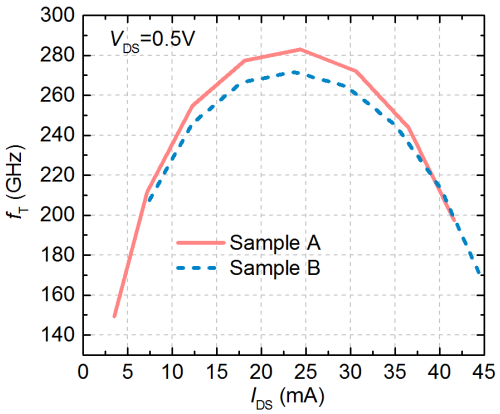

Fig. 3. Unity current gain frequency f_T versus I_{DS} at V_{DS} = 0.5 V for 50 nm gate (2 × 50) µm devices measured at 300 K.

transconductance g_{Mi} and gate-source capacitance C_{GS} are slightly higher for split A as a result of the more pronounced gate sinking resulting in smaller gate-to-channel distance. Although simultaneous increase in both g_{Mi} and C_{GS} should not have an impact on f_T, process split B shows a decreased f_T as a consequence of increased access resistances R_S and R_D due to the long gate passivation step performed at higher temperature (1°h at 250°C for process split B versus 1°h at 180°C for process split A).

DC and RF measurements performed at 15 K also reflect the same trends, as presented in Figures 4 and 5.

DISCUSSION

The effect of thermal annealing on diffusion depth of a Pt/Ti/Pt/Au gate in and AlInAs/GaInAs/InP HEMTs was in detail investigated versus annealing time [5] and annealing temperature [6]. It was demonstrated that the major part of diffusion process happens within first 10 minutes of annealing given that the temperature is high enough to enable diffusion process. However, we have demonstrated that despite even longer annealing time at the identical temperature of 250°C, the ALD process split does not feature a fully reacted Pt gate.

Results presented here suggest that annealing ambient and the thermal ramp rate have a significant influence on the device final characteristics. In order to investigate more thoroughly, one additional sample (C) was processed with gate sink-in performed in RTA, with the identical thermal ramp rate and temperature as for the process split A, but without the flow of the forming gas. Figure 6 shows the DC output and transconductance characteristics measured at 300 K for 2 × 50 μm HEMTs with a gate length of L_G = 50 nm.

The devices from sample C exhibit values for threshold voltage V_{th} and DC transconductance g_M in between measured values for split A and split B as seen in figure 6. The measured

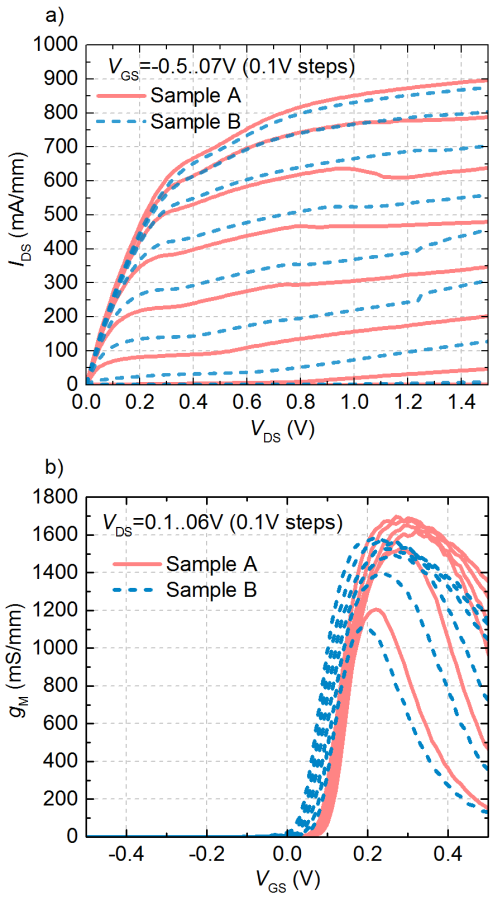

Fig. 4. (a) DC output and (b) transconductance characteristics of fabricated 2 × 50 µm HEMTs with gate length of 50 nm measured at 15 K.

gate leakage current is also higher compared to split A, but

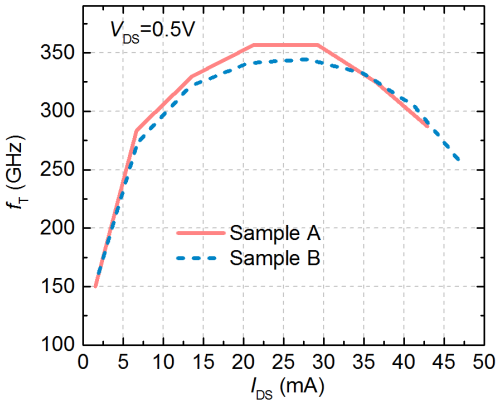

Fig. 5. Unity current gain cutoff frequency f_T versus I_{DS} at V_{DS} = 0.5 V for 50 nm gate (2 × 50) µm devices measured at 15 K.

lower compared to split B. These measurements imply that both the ambient and the thermal ramp have a crucial role for Pt gate sink-in.

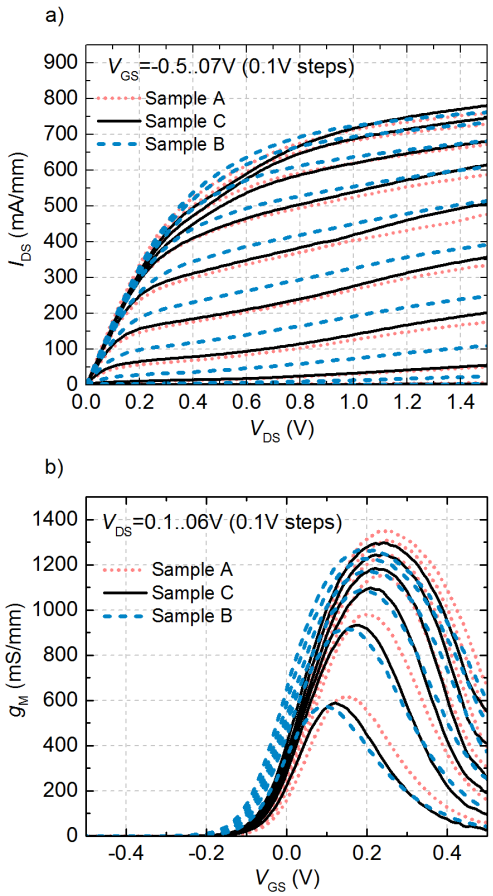

Fig. 6. (a) DC output and (b) transconductance characteristics of fabricated 2 × 50 µm HEMTs with gate length of 50 nm measured at 300 K.

RF measurements show de-embedded f_T for sample C within values extrapolated for split A and B. The small-signal equivalent circuit extraction shows that the values for intrinsic small-signal transconductance g_{Mi} and gate-source capacitance C_{GS} are among the values obtained for process splits A and B, suggesting that the gate sink-in depth for sample C is in between diffusion depths for split A and B. Access resistances R_S and R_D are only slightly higher for sample C compared to sample A due to the metal contact oxidation that takes place at high temperatures without the flow of the forming gas.

CONCLUSIONS

We investigated the impact of three different gate sink-in procedures on the DC and RF performance of AlInAs/GaInAs/InP HEMTs. The results indicate that both the forming gas atmosphere and the thermal ramping play key roles in the gate sink-in process. Despite the same final gate sink-in temperature of 250°C, and an effectively longer annealing time for the ALD split, the Pt sink-in reaction is incomplete. Sink-in performed in the RTA with the same

thermal ramping but without forming gas ambient also results in only partial diffusion. As a consequence, the gate contacts are further away from the channel making the threshold voltage (V_{th}) more negative and decreasing the maximum transconductance and gate current.

RF measurements show slightly higher cutoff frequency f_T for the devices from sample A, annealed in the RTA with the forming gas flow, despite simultaneously increased g_m and C_{gs} owing to the Ohmic contact degradation for both splits B and C. Observed increase in access resistances is a result of enhanced oxidation of metal contacts due to the long gate passivation step performed at higher temperature for split B, and due to the gate annealing in non-reducing atmosphere for split C.

ACKNOWLEDGEMENTS

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ACRONYMS

HEMT: High Electron Mobility Transistor
RTA: Rapid Thermal Annealer
ALD: Atomic Layer Deposition
MBE: Molecular Beam Epitaxy