None-Doped InGaP/GaAs Hetero-Junction p-channel FET

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Abstract

We have a demonstrated a GsAs monolithic microwave integrated circuit (MMIC) using a none-doped InGaP/GaAs Hetero-Junction p-channel field effect transistor (FET). We previously released enhancement- and depletion-mode (E/D mode) AlGaAs/InGaAs hetero-junction field-effect transistors (HJFET) that use electrostatic discharge (ESD) protection diodes. We optimized the device structure and epi growth conditions for both the ESD protection diode and p-channel FET. The structure of the p-channel FET is abnormal, but its fabrication process is very simple without an additional mask, and the ESD protection diode retains its function.

First, we used the p-doped channel, but the pinch-off voltage was difficult to control because of surface damage. Thus, a none-doped InGaP/GaAs hetero-junction was designed for the channel layer of the p-channel FET with support from epi venders. The none-doped InGaP/GaAs hetero-junction structure generates the hole carrier under biased. The pinch-off voltages of p-channel FET are very suitable.

We have been mass-producing switch integrated circuits (SW ICs) with a logic circuit that uses a none-doped InGaP/GaAs Hetero-Junction p-channel FET since 2009.

INTRODUCTION

We previously reported E/D mode AlGaAs/InGaAs HJFETs with ESD protection diodes on them in MANTECH 2009 [1]. HJFETs enabled the mass production of switch/low-noise-amplifier integrated circuits (SW/LNA-ICs) with sufficiently small chips, high ESD, and low cost to make them competitive with Si devices. However, recent MMICs require a more complicated logic circuit to improve their performance, and we are limited to producing higher level circuits by using E/D mode HJFETs. To solve this problem, we attempted to add a p-type channel FET for the logic together with an ESD protection diode and E-D mode HJFETs in the same wafer.

Complementary GaAs technologies have already been developed by using the conventional p-channel FET structure [2-3]. This paper presents a none-doped InGaP/GaAs hetero-junction p-channel FET. First, we review the structure and process integration of our p-channel FET. Next, we show how to improve its characteristics. Finally, we present an application using this p-channel FET.

STRUCTURE AND PROCESS INTEGRATION OF P-CHANNEL FET

Our developed p-channel FET consist of PIN diodes, which are formed on a wafer with E/D-mode AlGaAs/InGaAs HJFETs, as shown in Fig. 1. The E/D-mode HJFETs are formed on a conventional double-doped and double-hetero-junction epi-structure [4].

p+GaAs (contact layer), InGaP (Etching stopper layer), InGaP/GaAs (p-channel layers), and n+GaAs (gate layer) are grown by metal-organic vapor-phase epitaxy (MOVPE). An n+GaAs layer is also used as the contact layer of n-channel FET.

To fabricate the p-channel FET, first, the p+GaAs, InGaP, GaAs, and InGaP layers are etched. After isolation by ion implantation, the p+GaAs layer and n+GaAs layer are etched at the same time to format the p-channel and n-channel surfaces. Source-drain contacts of p-channel FET on p+GaAs are formed by Pt/Ti/Pt/Au the same as the gate electrode of the n-channel FET. Gate electrodes of the p-channel FET on n+GaAs are formed by Au/Ge/Ni/Au the same as source-drain contacts of the n-channel FET. The structure of the p-channel FET is a back-gate pn junction FET (JFET) similar to the JFET of Integrated HBT and FET devices (BiFET) [5]. No additional masks are added to the existing HJFET production process flow.

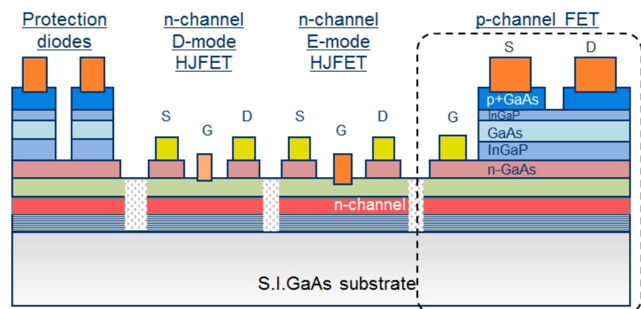

Fig. 1. Schematic cross section of device structure.

At the initial stage of this development, we simply added the p-doped GaAs channel on the top, but the pinch-off voltage was very difficult to control because of the surface damage of the channel. After several trials, we finally

developed an easily and stably controlled p-channel FET using non-doped InGaP/GaAs hetero-junction with support from epi venders. Free holes are generated under biased in the region close to the interface in the non-doped GaAs layer due to the interface charge of the InGaP/GaAs system, coming from polarization of InGaP.

CHARACTERISTICS OF P-CHANNEL FET

We measured DC characteristics of the E-mode p-channel FET at room temperature. Fig. 2(a) shows the Ids-Vgs characteristic of the p-channel FET. The Vth of the p-channel FET is -0.61 V at Ids=-100 µA/mm and Vds=-1.0 V. The leakage current at Vgs=0 V is around 10 nA/mm.

Fig. 2(b) shows the Ids-Vds characteristic of the p-channel FET at room temperature. The Vgs step is from -1.0 V to -0.5 V at 0.1 V steps. The Ron is 110 ohm/mm.

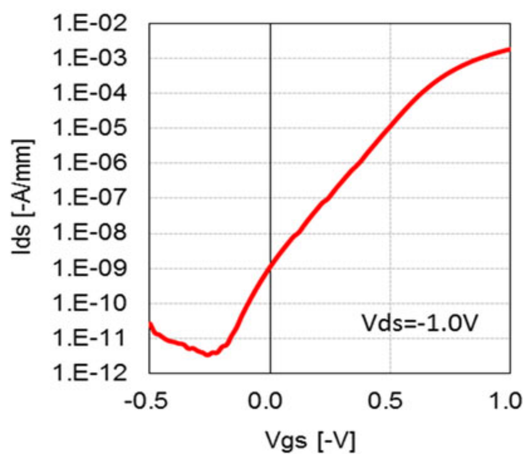

Fig. 2(a). Ids-Vgs curve of p-channel FET.

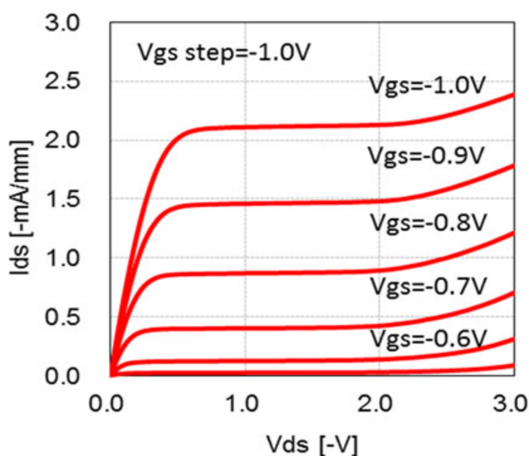

Fig. 2(b). Ids-Vds curve of p-channel FET

Fig. 2(c) shows the gate forward characteristic of the p-channel FET at room temperature. The gate turn-on voltage (Vf) is -1.0 V. The Vf is made higher by the pn junction gate.

Fig. 2(d) shows the gate reverse characteristic of the p-channel FET at room temperature. Gate leakage current is around 50 nA/mm, and breakdown voltage is 10 V. Breakdown voltage is decided by the thickness of the p-channel InGaP/GaAs layer.

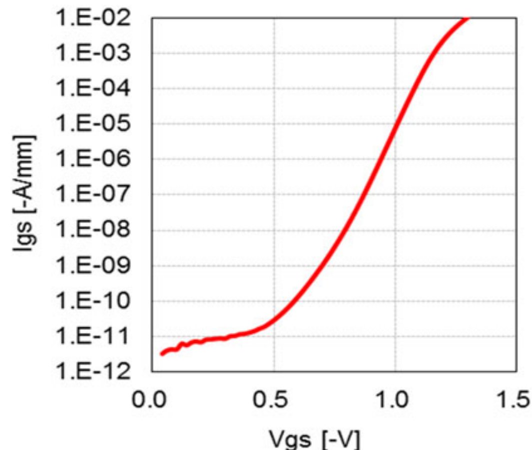

Fig. 2(c). Igs-Vgs (forward) curve of p-channel FET.

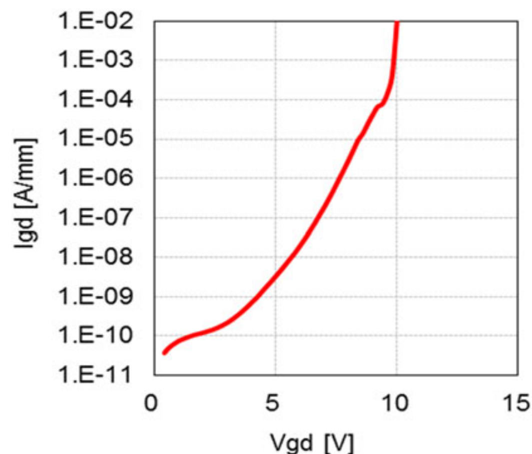

Fig. 2(d). Igd-Vgd (reverse) curve of p-channel FET.

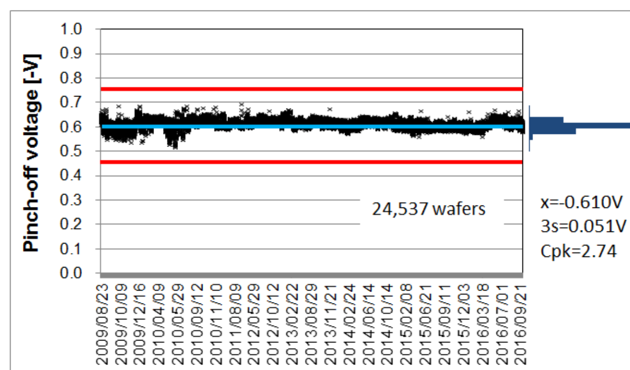

Fig. 3. Trend chart of pinch-off voltage of p-channel FET.

Fig. 3 shows the trend chart of pinch-off voltage of p-channel FETs from 2009 to 2016 for mass production of 24,537 wafers. Pinch-off voltages of p-channel FET are very suitable in spite of two epi venders being used.

INVERTER PERFORMANCE

Fig. 4 schematically shows a complementary inverter circuit constructed by using a p-channel FET and an E-mode HJFET. Fig. 5 shows the temperature characteristics of static voltage transfer for the complementary inverter circuit. Turn-off voltage is suitable for the temperature due to a complementary FET being used.

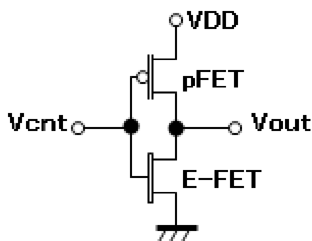

Fig. 4. Schematic of inverter.

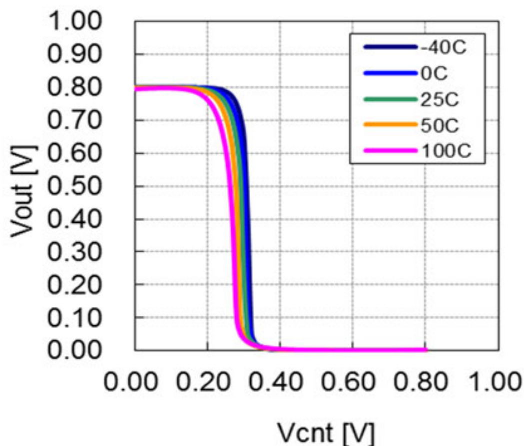

Fig. 5. Temperatures of static voltage transfer of inverter circuit.

DEMONSTRATION OF APPLICATION

Our p-channel FET technology was applied to MMIC products such as switches (SWs). Fig. 6 shows a photograph of a single pole double throw (SPDT) SW (NJG1681) for LTE/UMTS/CDMA/GSM applications. NJG1681 features very low insertion loss (0.16 dB), high isolation (30 dB), and excellent linearity performance (P-0,1 dB=36 dBm) down to 1.8 V control voltage at up to 2.7 GHz. NJG1681 uses ESD protection devices to achieve excellent ESD performances (MM>200 V, HBT>2000 V). No radio frequency (RF) ports require DC blocking capacitors. The P-channel FET was used at a negative voltage control circuit. Thus, we can realize a small and high performance SWs by using our p-channel FET.

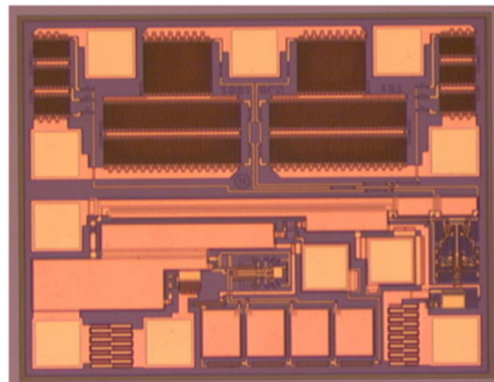

Fig. 6. Photograph of SPDT SW (NJG1681).

CONCLUSION

We developed an E-mode p-channel FET formed on a wafer with E/D-mode HJFETs and protection diodes. The p-channel FET has a none-doped InGaP/GaAs channel and a unique device structure. No additional mask is needed to realize the p-channel FET. Therefore, the pinch-off voltage of the p-channel has been very suitable for seven years in spite of two epi venders being used. We produced a high performance MMIC by using the p-channel FET.

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ACRONYMS

GaAs: Gallium Arsenide
InGaP: Indium Gallium Phosphide
MMIC: Monolithic Microwave Integrated Circuit
ESD: Electrostatic Discharge
HJFET: Hetero-Junction Field-Effect Transistors
JFET: Junction Field-Effect Transistors
BiFET: Integrated HBT and FET devices
SPDT: Single Pole Double Throw