High Performance Normally-Off Operation p-GaN Gate HEMT with Composited Barriers Structure Design

Yi-Sheng Chang[1], Bo-Hong Li[1], Hsiang-Chun Wang[1], Hsien-Chin Chiu[1], Rong Xuan[2], Chih-Wei Hu[2], and Jung-Ruey Tsai[3]

[1] Department of Electronics Engineering, Chang Gung University, Taiwan, R.O.C.
[2] Technology Development Division, Episil-Precision Inc, Taiwan, R.O.C
[3] Department of Photonics and Communication Engineering, Asia University, Taiwan, R.O.C.
e-mail: hcchiu@mail.cgu.edu.tw, Phone: +886-3-2118800 # 3645

Keywords: HEMTs, 2-DEG p-GaN, Enhancement mode, Current collapse and Dynamic *R*ON

Abstract

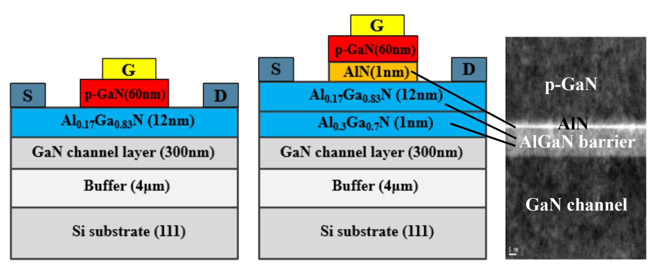
In this work, a novel composited barriers design of high electron mobility transistors (HEMTs) with normally-off operation mode composed of p-GaN/AlN/AlGaN/AlGaN/GaN structure was fabricated. Compared to the conventional p-GaN/AlGaN/GaN structure of HEMTs, the composited barriers can effectively reduce the plasma-induced damage leading to the reduction of the increased dynamic ON-resistance (R_{ON}) after pulsed current-voltage stress operating. The excellent electrical characteristics of maximum drain current density and low subthreshold swing (S.S) of 320 mA/mm and 137 mV/dec, respectively, can be obtained in the proposed composited barriers p-GaN gate structure of HEMT.

INTRODUCTION

In recent decades, GaN-based high electron mobility transistors (HEMTs) have attracted much attention in the high-voltage, high-power and device-switching applications due to their excellent material properties, such as high breakdown voltage, high switching frequency, low-channel resistance, and so forth. However, the normally-on operation characteristics of the conventional GaN-based HEMTs are usually not preferred in power electronic applications mainly due to their inconvenient operation and unavoidable power consumption. Thus, several researches have been proposed to realize the normally-off operation characteristics of the AlGaN/GaN HEMTs using various structures such as ultrathin barrier [1-2], gate-recessed HEMTs structures [3-4], triple cap layer and high-k gate dielectrics [5], deep-recess V-gate technology [6], and using a p-type capping layer [7] to reduce the concentration of two-dimensional electron gas (2DEG) in the channel of devices. However, the drain current density is much lower than normally-on devices, which results in the higher dynamic R_{ON} during device operation. Especially, these issues will be further degraded after electrical stress operating to cause the deterioration of device reliability. In the work, a novel composited barriers structure using AlN capping layer in the p-GaN Gate HEMT with normally-off operation is proposed to improve the drain current density and on-state resistance after the pulsed current-voltage (I-V) stress testing.

DEVICE STRUCTURE AND FABRICATION

Fig. 1 shows the schematic of the conventional and proposed structure with composited barriers design in the p-GaN gate HEMTs. For the proposed p-GaN HEMTs, the epitaxial layers were grown on a Si (111) p-type substrate by metal organic chemical vapor deposition (MOCVD) which are composed of a 4µm-thick buffer layer, a 300 nm GaN channel, a 1nm $Al_{0.3}Ga_{0.7}N$ barrier, a 12 nm $Al_{0.17}Ga_{0.83}N$ barrier, a 1nm AlN capping layer and a 60 nm p-type GaN gate layer (Mg doping concentration = 3×10^{19} cm^{-3}). The device fabrication started from defining the mesa area by reactive ion etching (RIE). The p-GaN island was formed by RIE with the etching gas BCl_3 + CF_4. Ohmic contacts was prepared by the electron beam evaporation to perform a multilayered Ti/Al/Ni/Au (25/120/25/150 nm) sequentially, followed by rapid thermal annealing (RTA) at 875 °C for 30 s in a nitrogen-rich ambient. After the gate region of Ni/Au (25/120 nm) metal layer was deposited by electron beam evaporator. Finally, a 200 nm-thick SiO_2 surface passivation layer was deposited via E-beam evaporator. The lengths of gate-to-source (L_{GS}), gate (L_G), gate-to drain (L_{GD}) are 2, 2 and 3µm, respectively. The width of device (W) is 50µm.



(a) Structure A (b) Structure B

Fig. 1. Schematic structures of the p-GaN HEMTs with the (a) conventional barrier and (b) composited barrier design.

Results And Discussion

Fig. 2 shows the energy band diagram distributions of different structures. Compared with the conventional p-GaN HEMT, it clear suggests the insertions of the wide band gap 1-nm AlN cap layer and the 1-nm $Al_{0.3}Ga_{0.7}N$ barrier in the proposed device can increase higher effective ΔE_C and polarization effect in the channel, respectively.

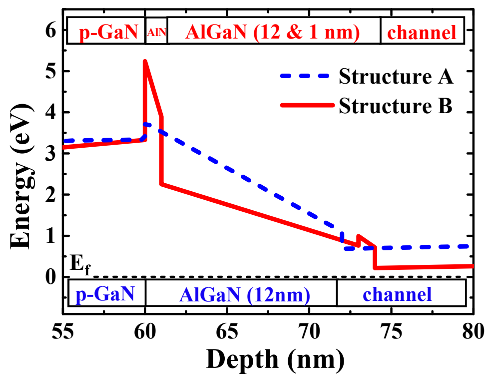


Fig. 2. The conduction band energy distributions of the structure A and B.

Fig. 3 displays the transfer characteristic conventional and proposed composited barrier structures at V_{DS}=10 V. It clearly suggests that the threshold voltage can be decreased from 2.1 to 1.7 V due to more 2DEG concentration in the channel caused by the increase of polarization effect caused by the insertion of 1-nm-thick $Al_{0.3}Ga_{0.7}N$ layer, described in Fig. 3. Furthermore, the off-state leakage can be improved by higher than one order of magnitude significantly in the proposed structure mainly due to the composited barriers of insertion of 1nm AlN capping layer. As a result, the proposed structure of HEMT shows an excellent S.S value of 167 mV/dec.

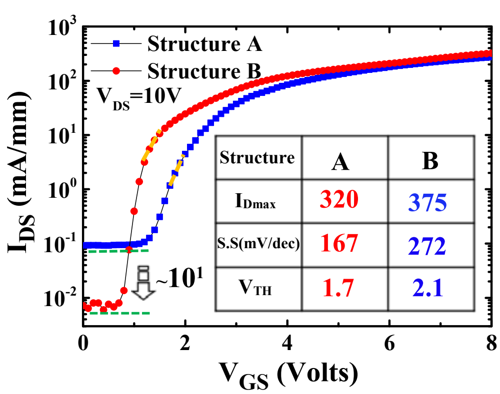


Fig. 3. The transfer characteristic of the structure A and B.

For the evaluation of current collapse behavior, the applied pulsed waveforms and timing diagrams are shown in Fig. 4. The device is switched from the off state with a V_{GSQ} of 0 V and V_{DSQ} is ranging from 0 to 200 V with a voltage step of 50V. The of V_{GS} and V_{DS} with pulse width of V_{GS} and period of V_{DS} are 2 µs and 200 µs. These transient OFF-to-ON switching I-V characteristics of the device is performed with an AMCAD pulsed I-V system.

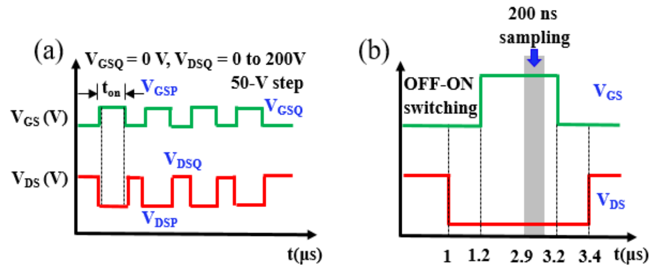


Fig. 4. Pulsed I-V characterization: (a) waveforms of V_{GS} and V_{DS}; (b) timing diagrams of V_{GS} and V_{DS} with periods of OFF-to-ON switching (200 ns) and sampling time (200 ns) in ON-state.

Fig. 5 plots the DC and pulsed I_D-V_{DS} characteristics in the conventional and proposed structures of devices. The larger saturation current after stress is due to the field-assisted electron de-trapping from the traps at the drain-side gate edge. It clear suggests the degradation of I_{DS} can be improved by approximately 10% in the structure B which implies the insertion of AlN capping layer can effectively reduce the generation of charge trapping states during the pulsed I-V stress periods.

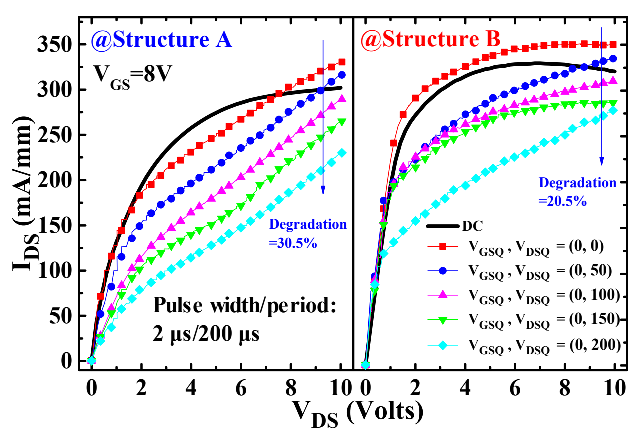


Fig. 5. Pulsed I_D-V_{DS} characteristics (with DC) were extract from quiescent bias stress of (V_{GSQ}, V_{DSQ}) = (0 V, 0—200 V, step= 50 V) with pulse width/period of 2 µs/200 µs.

Fig. 6(a) shows dynamic on-state R_{ON} behaviors in the conventional and proposed structures of HEMTs after pulsed I-V stress. It is clear that the conventional structure of device severely suffers from the plasma damage induced current collapse during pulsed I-V stress periods. Fig. 6(b) shows the dynamic on state current divided by static state current ratio. It reasonably suggests that the insertion of AlN capping layer can depress the generation plasma-induced damage leading to the decrease of the degradation of dynamic R_{ON} and dynamic on state current divided by static state current ratio during pulsed I-V stress.

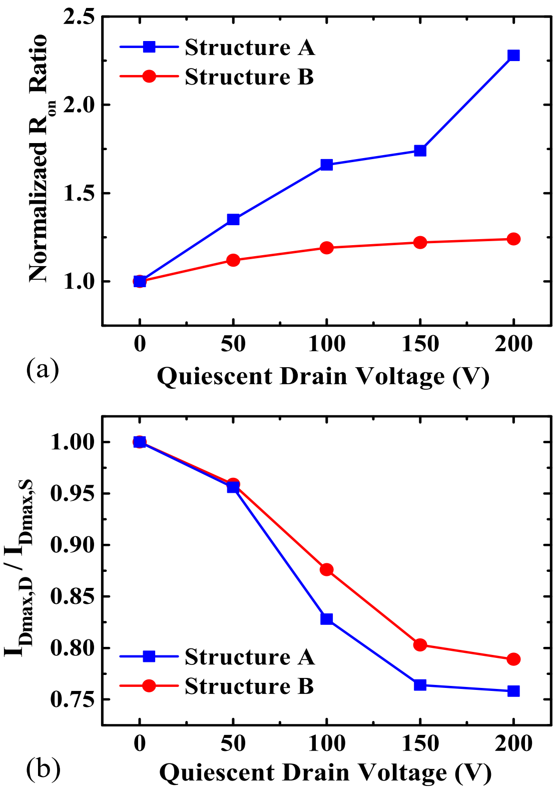


Fig. 6. With quiescent drain bias stress voltage of (a) Dynamic R_{ON} ratio and (b) $I_{Dmax,D}$ / $I_{Dmax,S}$ ratio.

Conclusions

In this work, a novel structure of p-GaN HEMT was fabricated successfully. The decrease of threshold voltage suggests that the ability of gate control to channel is increased mainly due to more polarization effect induced more 2DEG concentration in the channel which is caused by the insertion of AlN capping and $Al_{0.3}Ga_{0.7}N$ layer. Additionally, the proposed HEMT significantly demonstrated that the plasma damage-induced in current collapse and dynamic on-state resistance can be improved by the composited barriers design using the insertion of AlN capping layer.

References

[1] F. Medjdoub, J. Derluyn, K. Cheng, M. Leys, S. Degroote, D. Marcon, D. Visalli, M. Van Hove, M. Germain, and G. Borghs, "*Low On-Resistance High-Breakdown Normally Off AlN/GaN/AlGaN DHFET on Si Substrate*," IEEE Electron Device Letters, Vol. 31, No. 2, February 2010.

[2] Y. Ohmaki, M. Tanimoto, S. Akamatsu, and T. Mukai, "*Enhancement mode AlGaN/AlN/GaN high electron mobility transistor with low onstate resistance and high breakdown voltage*," Jpn. J. Appl. Phys., vol. 45, no. 44, pp. L1168–L1170, Nov. 2006.

[3] T. Oka and T. Nozawa, "*AlGaN/GaN recessed MIS-gate HFET with high threshold- voltage normally-off operation for power electronics applications*," IEEE Electron Device Lett., vol. 29, no. 7, pp. 668–670, Jul. 2008

[4] Y. Okamoto, Y. Ando, T. Nakayama, K. Hataya, H. Miyamoto, T. Inoue, M. Senda, M. Hirata, K. Kosaki, N. Shibata, and M. Kuzuhara, "*High power recessed-gate AlGaN-GaN HFET with a field-modulating plate*," IEEE Trans. Electron Devices, vol. 51, no. 12, pp. 2217–2222, Mar. 2001.

[5] Masahito Kanamura, Toshihiro Ohki, Toshihide Kikkawa, Kenji Imanishi, Tadahiro Imada, Atsushi Yamada, and Naoki Hara, "*Enhancement-Mode GaN MIS-HEMTs with n-GaN/i-AlN/n-GaN Triple Cap Layer and High-k Gate Dielectrics*," IEEE Electron Device Letters, Vol. 31, No. 3, March 2010.

[6] Rongming Chu, Zhen Chen, Steven P. DenBaars, and Umesh K. Mishra, "*V-Gate GaN HEMTs With Engineered Buffer for Normally Off Operation*," IEEE Electron Device Letters, Vol. 29, No. 11, November 2008.

[7] Y. Uemoto, M. Hikita, H. Ueno, H. Matsuo, H. Ishida, M. Yanagihara, T. Ueda, T. Tanaka, and D. Ueda, "*Gate injection transistor (GIT)-a normally-off AlGaN/GaN power transistor using conductivity modulation*," IEEE Trans. Electron Devices, vol. 54, no. 12, pp. 3393–3399, Dec. 2007

Acronyms

HEMT: High Electron Mobility Transistor
2DEG: Two-Dimensional Electron Gas