Comparison of Floating and Grounded Substrate Termination on the Dynamic Performance of GaN-on-Si Power Transistors

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Keywords: GaN-on-Si, MIS-HEMTs, high voltage, substrate termination, dynamic performance, buffer trapping

Abstract

The dynamic performance of GaN MIS-HEMTs under both floating and grounded substrate terminations was studied. Devices with a floating substrate can deliver smaller dynamic degradation. To fully understand the difference resulting from terminations, comprehensive analysis of room temperature and high temperature dynamic performance with various structure designs was performed. The results suggest that the degradation is related to the electron trapping in GaN buffer, which can be suppressed by a floating substrate. However, the devices with floating substrate exhibited accelerated degradation under high voltage stress. One solution addressing the trade-off between dynamic performance and reliability of devices with different substrate terminations is to increase GaN buffer thickness of devices with a grounded substrate.

INTRODUCTION

With high-frequency switching and high-temperature operation capabilities, GaN-on-Si power transistors are attractive candidates for power electronics applications demanding high efficiency and power density, such as fast-charging power adapters and micro inverters [1, 2]. However, the adoption of these devices are challenged by reliability issues. For instance, charging/discharging of surface/interface traps or buffer traps during high-voltage switching operation could lead to an increase in the dynamic ON-resistance (R_{ON}) [3, 4].

Several approaches including surface pretreatment and advanced passivation scheme have been successfully developed to effectively suppress surface/interface trap density [5, 6]. However, high density buffer traps, resulting from intentional C doping for achieving high voltage blocking (e.g., 600 V) capability of GaN buffer, could also lead to severe device degradation. The influence of buffer trapping on the dynamic performance has been intensively studied by back-gating measurements with a negative bias applied on the Si substrate [7]. However, in practical applications, the viable options for substrate termination are probably limited to floating or being grounded.

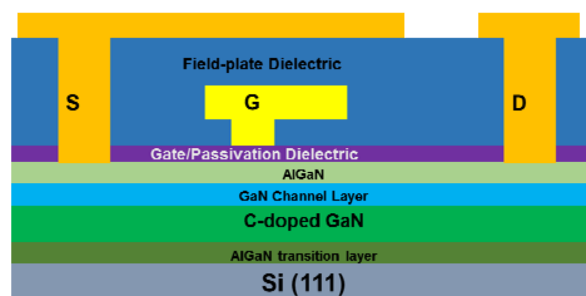

Fig. 1. Cross-sectional schematic of the 600-V D-mode MIS-HEMT. The device features gate- and source- terminated field plates.

In this work, the study on dynamic characteristics was focused on GaN MIS-HEMTs under both floating and grounded substrate terminations.

DEVICE FABRICATION

The GaN MIS-HEMT epi-structures consisted of a conductive Si substrate, an ~0.5 µm AlGaN transition layer, a few-micron C-doped GaN buffer layer (C-GaN), a 100 nm GaN channel layer, and a 25 nm AlGaN barrier layer. These devices also feature a gate-terminated and a source-terminated field plate. The cross-sectional schematic of the device structure is depicted in Fig. 1.

Devices for characterization were taken from five wafers representing different lots with detailed design splits as summarized in Table I. In the baseline lot (Lot-1), D-mode MIS-HEMTs were fabricated on GaN-on-Si wafers with a 3.5 µm GaN buffer layer doped at a carbon concentration of ~$7\times10^{18}/cm^3$. They were passivated with a high-temperature-grown LPCVD-SiN_x, as it can offer better dielectric reliability under high-voltage and high-temperature stress [8].

TABLE I
SUMMARY OF DESIGN SPLITS FOR DIFFERENT LOTS

Design Splits	Gate/Passivation dielectric	Field plate design	C-GaN thickness
Lot-1 (Baseline)	LPCVD-SiN_x	Design-1	3.5 µm
Lot-2	PECVD-SiN_x	Design-1	3.5 µm
Lot-3	LPCVD-SiN_x	Design-2	3.5 µm
Lot-4	LPCVD-SiN_x	Design-1	4.0 µm
Lot-5	LPCVD-SiN_x	Design-1	4.5 µm

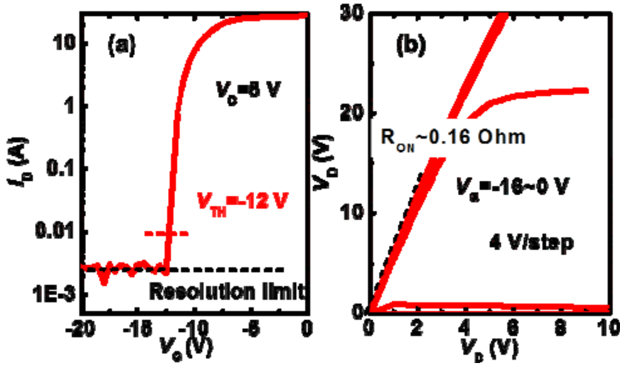

Fig. 2. (a) Transfer and output characteristics of a 600 V MIS-HEMT (Lot-1) with a gate width of 100 mm. The device exhibits a threshold voltage (V_{TH}) of -12 V at a drain current of 10 mA, and an R_{ON} of 160 mΩ; (b) OFF-state I-V characteristics of the device (Lot-1) with a floating substrate. The OFF-state breakdown voltage is larger than 600 V at a leakage current of 10 µA.

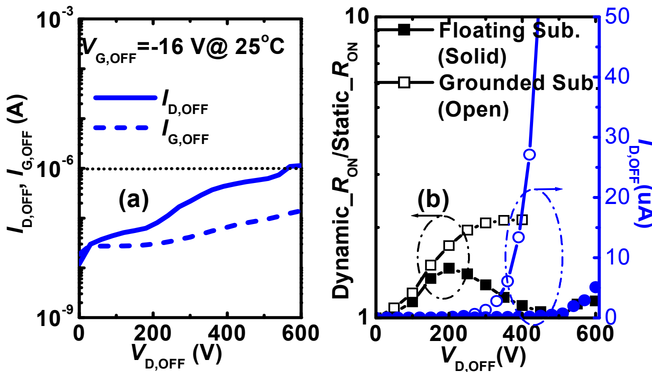

Fig. 3. Dynamic R_{ON} degradation and OFF-state leakage characteristics of the MIS-HEMTs (Lot-1) with floating or grounded substrate. The dynamic R_{ON}, measured at 100 µs after the high voltage stress, shows a clear correlation with the leakage current.

In lot-2, the devices were passivated with low-temperature-deposited PECVD-SiN_x after *in situ* NH_3 plasma pretreatment was conducted. This passivation scheme was proved to be efficient in reducing the surface/interface traps [9]. Compared with the baseline Lot-1, devices in Lot-3 have a different field plate design to suppress surface/interface trapping effect through electrical field modulation [10]. To further enhance blocking voltages, MIS-HEMTs in Lot-4 and Lot-5 were fabricated on wafers with thicker GaN buffers, which have C-doping concentration comparable with buffer in lot-1, while using the same baseline fabrication process as Lot-1.

RESULTS AND DISCUSSION

The fabrication of MIS-HEMTs feature a 2 µm gate-length, a 20 µm gate-to-drain spacing and a 100 mm gate width; their typical DC characteristics are shown in Fig. 2. The device exhibits a threshold voltage (V_{TH}) of -12 V at a drain current of 10 mA, an on-resistance of 160 mΩ corresponding to current rating higher than 10 A. The off-state breakdown voltage of the MIS-HEMT with a floating substrate is higher than 600 V at an off-state leakage of 10 µA (Fig. 3(a)).

The dynamic performance of devices was evaluated using Keysight N1267A HVSMU/HCSMU fast switch and B1505A power device analyzer. During the switching test, the devices were first held in a high voltage OFF-state for

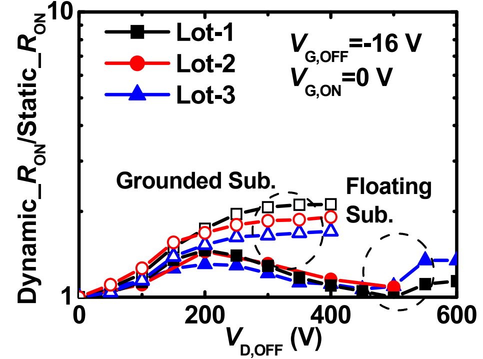

Fig. 4. Comparison of dynamic R_{ON} degradation of MIS-HEMTs with different passivation dielectric (Lot-2) or field plate design (Lot-3). Those devices show highly similar change of dynamic R_{ON} with $V_{D,OFF}$ when the substrate termination is the same.

30s. Then a simutaneously switching of devices' gate voltage (V_G) and drain voltage (V_D) to ON-state were achieved by turning on the switching FET in N1267A. The dynamic R_{ON} was evaluated at 0 V V_{GS} and 0.5 V V_{DS} bias at 100 µs after each switching. Typical dynamic performance of devices with floating or grounded substrate are shown in Fig. 3(b).

Devices with a floating substrate exhibits lower OFF-state leakage and smaller dynamic R_{ON} degradation.

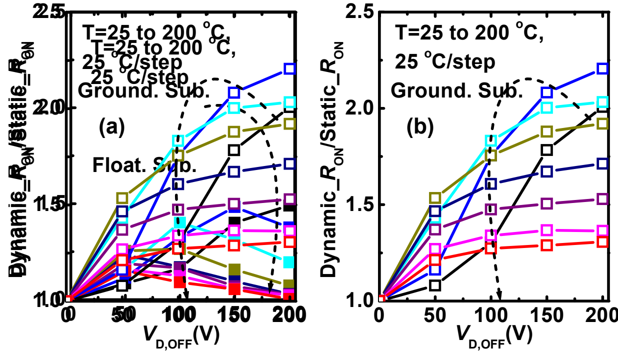

Fig. 5. Temperature dependent dynamic R_{ON} degradation of MIS-HEMTs (Lot-1) with (a) floating and (b) grounded substrate with an OFF-state stress up to 200 V. At higher temperatures, the dynamic degradation also exhibits a maximum value in terms of reduction (for floating sub.) or saturation (for grounded sub.) of R_{ON} with an increasing V_{OFF}. Meanwhile, the onset voltage of reduction/saturation becomes lower at high temperatures.

Moreover, similar trends in degradation were also observed for devices with different passivation or field plate design under both floating and grounded substrate terminations (Fig. 4). These results indicate that the interface/surface trapping might not a dominant factors for observed degradation. Therefore, the major reason is likely to be related to buffer trapping.

A closer examination of Fig. 4 reveals that the dynamic R_{ON} degradation of the MIS-HEMT with floating substrate exhibits a peak at around $V_{D,OFF}$ = 200 V and then it decreases at a higher $V_{D,OFF}$. This is because electron injecting/trapping in the GaN buffer through leakage paths is greatly offset by electron de-trapping, especially under high lateral E-field when the de-trapping process becomes dominant [11]. The degradation of dynamic R_{ON} in devices with grounded substrate, however, won't saturate until $V_{D,OFF}$ reaches 300 V. This "delay" is due to the much higher buffer leakage current in devices with grounded substrate, which could partially work against the de-trapping process.

The above-mentioned mechanism could also explain the observed device dynamic performance during high temperature switching operation, as shown in Fig. 5. When temperature increases, onsets of reduction in dynamic R_{ON} for devices on floating substrate and the saturation in dynamic R_{ON} for devices on grounded substrate exist, but shift to lower voltages (~50 V). It is well known that the de-trapping is a thermally accelerated process [3, 4, 7].

Although a floating substrate offers smaller degradation of dynamic R_{ON}, devices with floating substrate are more vulnerable to catastrophic failure (e.g., dielectric breakdown) compared to those on grounded substrate as

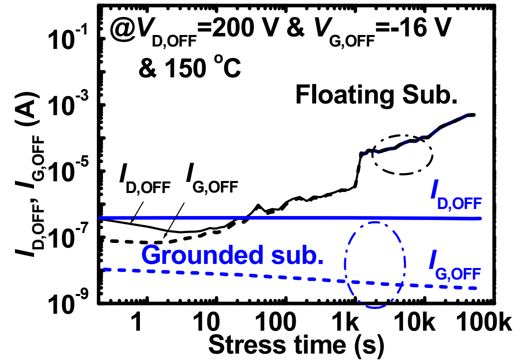

Fig. 6. $I_{D,OFF}$, $I_{G,OFF}$ degradation of a 600-V MIS-HEMTs (Lot-1) with $V_{D,OFF}$ = 200 V, and temperature = 150 °C. The device exhibits accelerated degradation with floating substrate termination.

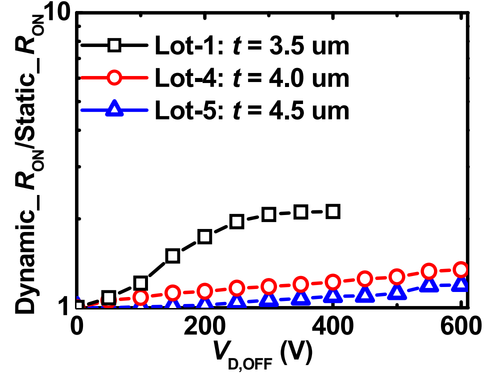

Fig. 7. Comparison of dynamic R_{ON} degradation of MIS-HEMTs with various buffer thicknesses (t). The dynamic performance is improved by suppressing vertical leakage induced buffer trapping.

shown in Fig. 6, because the grounding could serve as an additional field plate and thus avoid high potential in C-doped GaN buffer [12]. Therefore, there is a tradeoff between good dynamic performances (for which floating substrate termination is preferred) and enhanced device reliability (for which grounded substrate termination is preferred).

One solution to the dynamic R_{ON} of devices on grounded substrate that is inferior to that of devices based on floating substrate is to increase the GaN buffer thickness while keeping the substrate grounded during the operation. Fig. 6 indicates dynamic performance can be improved with a thicker buffer probably due to its suppression of the vertical electron injection into the GaN buffer.

CONCLUSIONS

GaN-on-Si MIS-HEMTs targeting at high-voltage and high-temperature switching applications show less degradation in dynamic R_{ON} under floating substrate termination compared with grounded substrate termination. The improved dynamic performance is highly related to the suppressed vertical electron injecting/trapping into GaN buffer. However, devices with floating substrate suffer increased risk of reliability issue, leaving substrate floating unlikely to be an applausive way to achieve stable device performance. On the other hand, improved dynamic performance could also be delivered by increasing GaN buffer thickness when substrate is grounded.

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ACRONYMS

MIS: Metal-Insulator-Semiconductor
HEMTs: High Electron Mobility Transistors
D-mode: Depletion-mode
LPCVD: Low-Pressure Chemical Vapor Deposition
PECVD: Plasma-Enhanced Chemical Vapor Deposition