Stacked Capacitors and Adaptive Manufacturing

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Keywords: MIM capacitors, IPD, GaAs backend, Adaptive Manufacturing

Abstract

Metal-insulator-metal (MIM) capacitors are important elements for power amplifier design, especially as part of an integrated matching network or IPD (integrated passive device) output matching network. Designers would like having higher precision capacitors but the lack of fuses makes post-final test trimming of the circuit impractical. In this work, we analyze and demonstrate MIM capacitor variation improvement based on the concept of adaptive manufacturing. Because the propose solution is fabricated using so-called "stacked" capacitors, it offers die size advantages over a fused based or "wiring in" type solution. Comparisons and analysis will be presented.

INTRODUCTION

Metal-insulator-metal (MIM) capacitor variation is often a critical feature for the RF performance of power amplifiers. In particular, second harmonic traps and output match capacitor variation can limit circuit yield. While solutions such as "trimming", commonly done in filter technologies [1,2], or wiring in different adjacent capacitors are possible [3], the first is impractical from a through-put perspective and the second would result in larger die. Another possible solution known as adaptive manufacturing [4] presents an interesting option for reducing capacitor variation and does not require extra mask space. The general concept of adaptive manufacturing is to measure a parameter at a point in the process before all metallization has been placed. Then different photomask plates are used to change the subsequent interconnect metals, and wire in different elements to adjust for the earlier measured values. The end result is the element is closer to the target value. The specific concept proposed here is to measure the bottom plate capacitor in the stacked capacitor and adjust the area of the top plate capacitor based on this measurement. The bottom plate capacitor can be tested prior to the deposition of a second capacitor plate over a second dielectric. The flow chart for this decision process is shown in Fig. 1. Since this adaptation is performed at a wafer level, with wafers queued to use the same mask plate, there is minimal hit to fab throughput.

Before applying adaptive manufacturing structures to MIM capacitors, the analysis began with the non-adapted

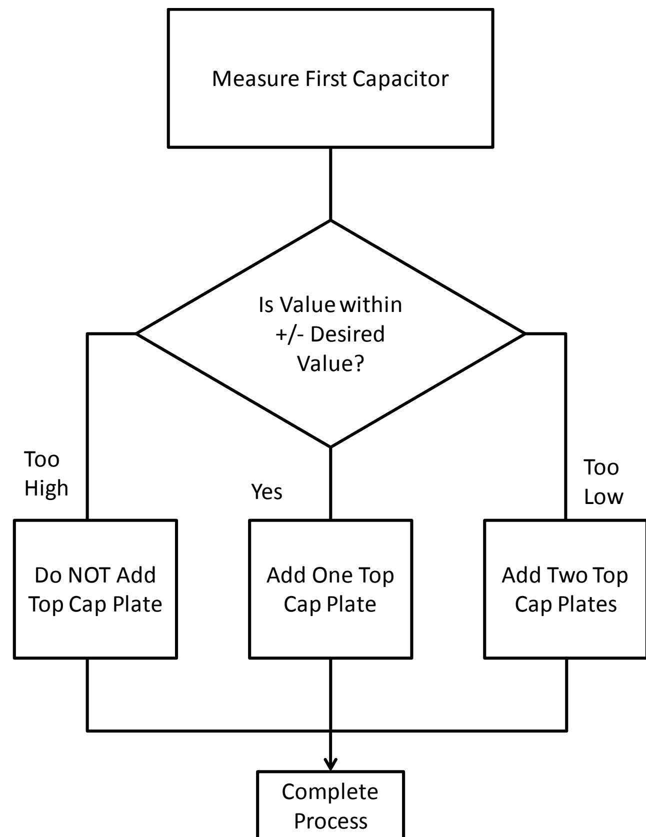


Fig. 1. Flow chart for adapting capacitors.

stacked capacitors. The components of capacitor variation for each of the capacitors in this process are shown in Table I assuming 3 standard deviations (3σ). It is noted that the variation of a stacked capacitor is better than an equivalent value single layer capacitor. The variation is smaller because the capacitors are in parallel and the variation is the root-mean-square value of the individual variation of the top and bottom capacitor plates. As an example, the variation of the bottom capacitor in the stacked capacitor has a variation of about 5.6%. The variation of the top capacitor (with thicker nitride) is around 3.93%. The resulting variation of the combined capacitor is about 4.8% which is based on measured values from about 275 wafers. Using a stacked capacitor instead of the bottom capacitor of the same value, improves the variation about 0.8%. From the partitioning, the

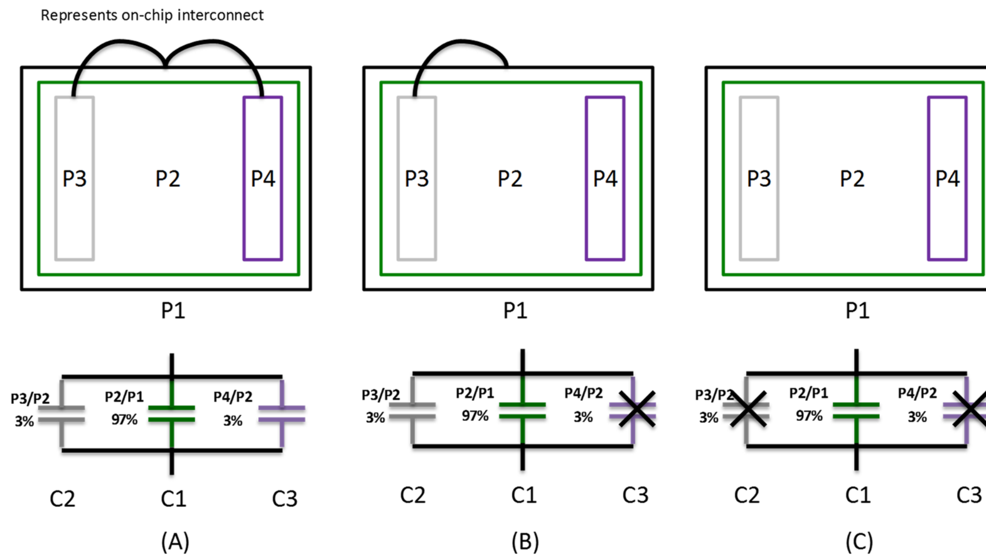
TABLE I
PARTITIONING OF VARIATION FROM CAPACITORS

Variation	Bottom Cap	Top Cap	Stack Cap
Within wafer variation (%)	2.65	2.06	2.36
Wafer to wafer variation (%)	3.06	2.54	2.69
Lot to lot variation (%)	3.8	2.42	3.19
Calculated total variation (%)	5.55	4.06	4.79
Measured total variation (%)	5.25	3.93	4.77

best variation we could achieve, by adapting the capacitors, is the across wafer variation. The MIM top single layer capacitor is not considered practical for the application due to the resulting capacitor's large footprint. The variation of wiring together side-by-side capacitors is the same as the variation of that capacitor assuming that they are large enough that geometrical effects can be ignored. As an application example, suppose we target a capacitance value of 1pF. The bottom plate would consist of a 0.97 pF capacitor based on the capacitance density (pF/mm^2) of the lower dielectric. The capacitance value of the lower cap is measured once the top plate of the bottom capacitor was formed. If the value is within the 3% of the target value (0.97 pF), then a 0.03 pF capacitor would be added on top (using a different metal deposition and a different dielectric that gives random variation relative to the first capacitor) to achieve the value of 1pF. If the measured capacitance density is too low (<target-3%), then an additional 0.03 pF (so 2x0.03 pF for the top cap) capacitor is wired in to push what would be failing cap values into the passing region. If the measured cap value was too high (> target +3%) then neither of the 0.03 top capacitors would be wired in. The wiring cases are shown schematically in Fig. 2. We later present measured data from our manufacturing line where these structures were fabricated. The adjustment (top) capacitors sit directly on top of the "main" capacitor body so it is space efficient.

Before these structures were fabricated, historical capacitor data was used to determine the expected improvement. As shown in Fig. 3, the variation of the nominal capacitor (nominal) was evaluated, and the capacitor adapted (mathematically) by wiring in side-by-side capacitors (adapted), stacked-cap (Nom_w_mim), and adapted capacitor using two MIM plates on top (adapted_w_mim). For the calculations, the data from the measured PCM sites in each field was used for the bottom, top, and stacked caps. This situation represents the best case, site-by-site adaptation. The adapted with MIM provided the best capability, as shown in Fig. 3. The 3σ capacitor variation drops from 5.5% to 4.2% for the stacked-cap adaptation (or 5.3% to 4.2% for the stacked capacitor to adapted).

For manufacturing purposes, queuing wafers is more practical so we evaluated wafer-by-wafer adaptation as shown in Fig. 4. The improvement is from 5.3% to 4.8% for the stacked capacitor approach. Considering the benefit of wafer by wafer adaptation on the percentage of sites outside the 3% range, there is a decrease in failed sites from 9.5% to



P2/P1 forms a first capacitor whose value is 97% of the desired value
P3/P2 or P4/P2 are second and third capacitors with value 3% of the desired value
When the measured value of C1 within the expected values (+/-3%), then C1+C2 (or C1+C3) forms the capacitor (B)
When the measured value of C1 less than 0.97x expected value, C1+C2+C3 forms the capacitor (A)
When the measured value of C1 more than 1.03x expected value, then C1 forms the capacitor (C)

Fig. 2. A representation of the wiring options for adapted capacitors.

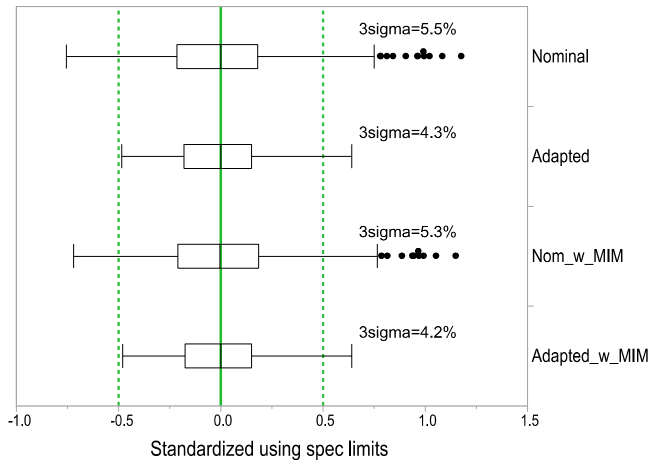


Fig. 3. Resulting capability box plots for Nominal (not adapted), adapted (side-by-side), nominal with MIM, and adapted with MIM (on top) for site by site adaptation (done by combining data for the individual capacitors, not measured. The percent variations are shown.

5.5%, which is a 4% improvement. This result can be explained by a cross-wafer variation causing some sites that should be corrected to not be corrected as well as correcting some sites that should not be corrected. For many applications, this is still a worthwhile improvement. Further tightening the adaptation limits improves the variation, but at the cost of having to adapt more wafers.

Finally, a test structure that implements the wiring scheme described in Fig. 1 was fabricated and tested to demonstrate that the top MIM plates provides the required +/-3% shifting of the capacitor is shown in Fig. 5. The measurement results are shown in Fig. 6. When the layout was developed, some wiring capacitance was inadvertently added to allow bottom plate immediately after top-plate formation. This was not accounted for in the wiring. Correcting for that capacitance, the top plates came very close to the target values as shown in Fig. 6.

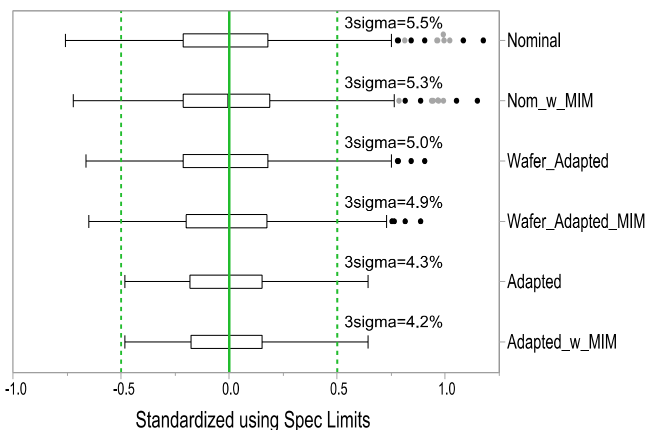


Fig. 4. Same data as for Fig. 3 but including wafer-by-wafer adaptation.

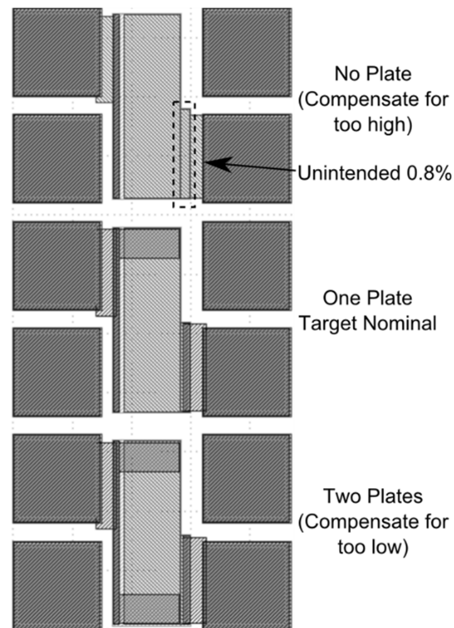


Fig. 5. Layout of test structure.

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Summary and Conclusions

Stacked capacitors allow for the opportunity of obtaining higher precision caps without any improvement in the actual manufacturing process. Analyzing and fabricating these structures, it was found that wafer by wafer adaptation improves ability to get within 3% by reducing the percentage of capacitors outside +/-3% from 9.5% to 5.5%. Site-by-site adaptation makes almost all capacitor variation within 3%.

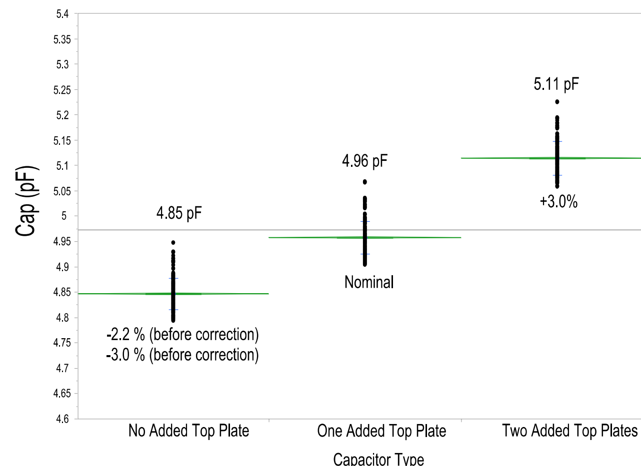

Fig. 6. Measurements of the three different wiring conditions for the capacitor from 12 wafers (3 wafers from 4 different lots) showing that the adaptive plates will give 3% correction.

However, site-by-site adaptation was shown not to be desirable for manufacturing throughput. An adaptive layout that has minimal impact on the total layout footprint has been demonstrated. It has been demonstrated that adaptive stacked capacitor construction can be implemented in a manufacturing process flow.

ACKNOWLEDGEMENTS

The authors would like to Denny Limanto for taking data on the manufacturing demonstration. Additionally, the authors would like to thank Qorvo NC Wafer Fab Operations for processing the wafers in this work.

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ACRONYMS

MIM capacitor: Metal-Insulator-Metal Capacitor
IPD: Integrated Passive Device
PCM: Process Control Monitor