Bias Stress-Induced Interfacial Instability Characterization in Oxidized SiC with Novel Non-contact Approach

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Abstract

We report a novel approach enabling comprehensive characterization of all four mechanisms of bias stress-induced interfacial instability in oxidized 4-H SiC: 1- oxide trap charging, 2- thermal activation, 3- interfacial trap generation, and 4- mobile ion drift. This is achieved with a novel application of corona-charge-Kelvin probe metrology. Corona charging provides a bias for non-contact C-V and a bias-stress with oxide field 1MV/cm to 3MV/cm, similar to that in SiC MOSFET bias stress, BS, and bias-temperature instability, BTI, testing. The entire stress-and-measure sequence is realized without fabrication of MOSFETs or MOS capacitors. We believe that the present approach, supplementing MOSFET testing shall prove beneficial for cost and time effective control of interfacial instability in SiC device development and manufacturing.

INTRODUCTION

Silicon carbide power MOSFETs are intended to operate at high temperatures and megavolts per cm gate bias range. Such conditions make MOSFETs susceptible to bias and temperature induced instability of the threshold voltage and reliability of the gate oxide. In a recent review Lelis et al. [1] discuss complex physical mechanisms of instability such as the near-interfacial oxide-trap charging via direct tunneling and the thermal activation effect. A review by Liu et al. [2] points out the significant effects of oxidation condition and post oxidation passivation treatments on the bias and temperature induced instability. It is apparent that engineering and understanding of the next generations of SiC/SiO_2 interfaces could benefit from new characterization capabilities.

Experimental instability results reported in literature have been obtained primarily from I-V MOSFET measurements of the positive and negative BTI of the threshold voltage. Habersat and Lelis [3] reported the benefits of C-V measurements on MOS SiC/SiO_2 capacitors whereby the bias stress effect on C-V characteristics exhibited instability features similar to results observed in I-V MOSFETs. The first observation of interfacial instability in SiC/SiO_2 performed with the non-contact C-V corona charge-Kelvin technique was reported by Oborina and Hoff [4]. The goal of the present work was to achieve comprehensive characterization of instability mechanisms with commercial non-contact corona-Kelvin tools recently developed by Semilab SDI for SiC and other wide-bandgap semiconductors [5]. Such a non-contact C-V SiC tool was also used in recently reported photo-assisted interface characterization that focused on slow charging-discharging processes involving interface traps [6].

Slow interface charging discussed in ref [6] for n-type oxidized SiC is illustrated in Fig. 1a,b. In a negative charge sweep from accumulation to depletion, the interface traps discharge via electron thermal emission to the conduction band shown in Fig. 1a. For deep traps possible in wide-band gap SiC, the large E_C-E_1 can make this process very slow. The reverse process, i.e. the filling of interface traps via electron capture, requires electron transfer over the surface barrier, qV_{SB}. A positive charge step toward flatband, $qV_{SB}\rightarrow 0$, facilitating efficient electron capture is shown in Fig. 1b as a transition to E_1. In photo-assisted measurements, illumination in deep depletion is used to empty deep interface traps. A subsequent positive charge sweep causes electron capture and hole emission shown in Fig. 1b that can significantly shift C-V characteristics in depletion [6].

The present instability measurement was performed without photo-assisted illumination. Contributions from interface state charging was further reduced by analyzing instability based on stress-induced voltage shift of C-V at flatband and in accumulation conditions.

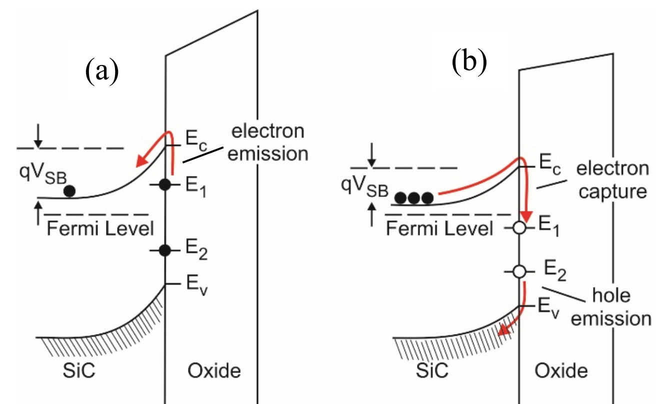

Fig. 1. Slow interface state charging processes of electron emission and capture and hole emission for n-type oxidized SiC.

EXPERIMENTAL RESULTS AND DISCUSSION

In the non-contact corona-Kelvin technique the corona discharge in air deposits precise increments of charge ΔQ_C and Kelvin probe measures the corresponding surface voltage increments ΔV. In 2015 the constant surface potential corona charging method was introduced, enabling precise charging over wider voltage range beneficial for characterization of wide bandgap semiconductors [7]. In present study corona charging is used for two purposes: 1- it creates a charge bias for noncontact differential capacitance measurement $C = \Delta Q_C / \Delta V$ giving static capacitance-voltage characteristic C-V where $V = \Sigma \Delta V$, and 2- larger doses of charging enable to apply charge controlled stress across dielectric in analogy to bias voltage controlled stress in MOS and MOSFETs.

Corona application 1 is essential for multiparameter electrical characterization of dielectrics, interfaces, and semiconductor materials [5]. Corona-Kelvin uses 6 mm diameter uniform charging spot at selected position of the wafer. Surface voltage is measured at the spot center with 2 mm diameter vibrating electrode of the Kelvin probe. The corona-Kelvin C-V characteristics shown in Fig. 2 were measured on a 6 inch diameter wafer of n-type epitaxial 4H-SiC with 45 nm thick SiO_2. Corresponding electrical parameters are listed in Table 1.

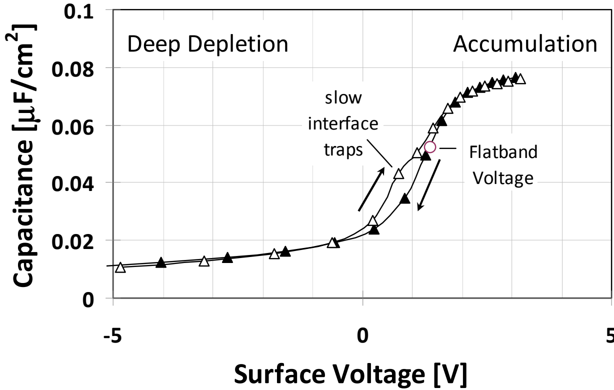

Fig. 2. Non-contact corona-Kelvin C-V characteristics measured in low corona charge bias range.

TABLE 1.
ELECTRICAL PARAMETERS DETERMINED WITH CORONA-KELVIN C-V FOR SAMPLE IN FIG. 2.

Parameter	Value
N_D [cm^{-3}]	9.13E+15
C_{OX} [nF/cm^2]	78.32
EOT [nm]	44.11
V_{FB} [V]	1.38
Q_{TOT} [q/cm^2]	1.43E+11

Characteristics in Fig. 2 were measured for positive and negative corona charging sweeps in the low bias range, without generating oxide trap charging effects and corresponding instability. Small hysteresis in the positive charge sweepseen in Fig. 2 is caused by slow interface trap charging via electron trapping transitions illustrated in Fig. 1b. To avoid this effect further analysis is based on negative sweep C-V characteristics as the one shown in Fig. 2 for the initial pre-stress condition.

The present study was done only for n-type SiC and instability results are reported for one way positive bias-stress. As required by instability monitoring procedures [1], post stress C-V characteristics were measured with a bias sweep in the direction away from the previous bias stress, i.e., with negative corona charging sweep. The presently used one-way positive bias-stress and negative sweep measurement sequence is illustrated in Fig. 3. The negative pre-stress initial C-V characteristic serves as a reference for instability quantification.

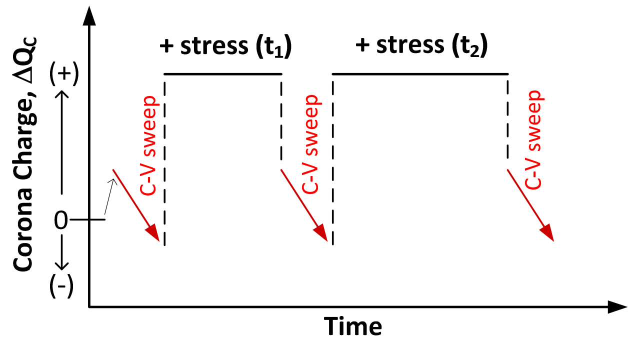

Fig. 3. Stress and measure sequence for one way positive corona bias stress and C-V sweep.

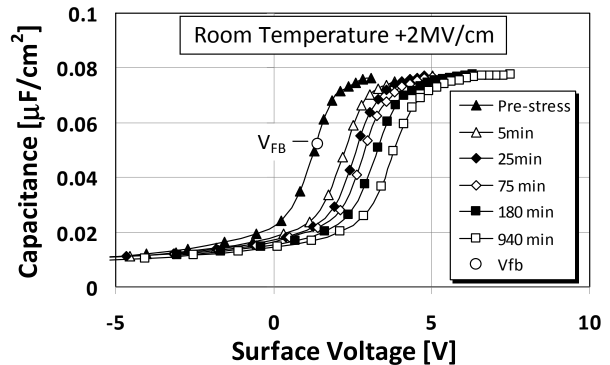

Fig. 4. C-V shifts induced by sequential one-way corona bias stress with increasing stress time.

Cumulative post-stress C-V results correspond to consecutive room temperature +2 MV/cm bias-stressing at the same wafer site with increasing stress time intervals. Time in Fig. 4 represents cumulative stress time. The evident

result of corona bias-stress is a practically parallel C-V shift in a positive direction. Positive shift corresponds to negative charging of near-interface oxide traps. The flatband voltage shift, ΔV_{FB}, from Fig. 4 is shown in Fig. 5 vs. stress time. This important result demonstrates logarithmic dependence on cumulative stress time consistent with literature data for SiC MOS and MOSFET instability. It also agrees with a direct tunneling mechanism of oxide trap charging [1]. In the tunneling oxide trap charging model the logarithmic stress time dependence of the voltage shift is a consequence of tunneling to traps positioned further from the interface [1].

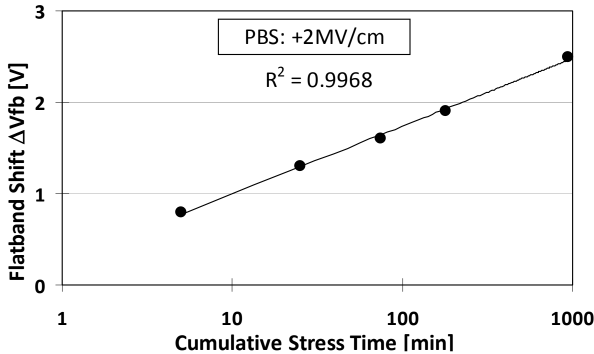

Fig. 5. Logarithmic stress time dependence of corona bias stress-induced flatband shift based on Fig. 4.

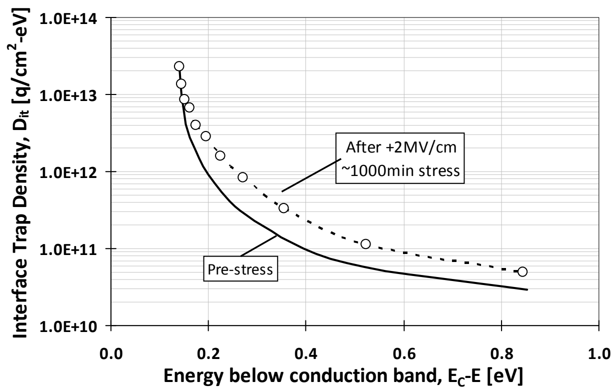

Fig. 6. D_{it} spectra showing corona stress induced interface trap density.

The dominant effect in Fig. 4 seems to be a translation of C-V curves analogous to MOS C-V instability results reported in Ref. 3. This together with very good ΔV_{FB} linearity with log-time implies no significant creation of the interface traps. We have examined this aspect and found that for long times the positive bias stress induces small, but measurable C-V stretch-out indicative of stress induced interface traps. From the D_{it} spectra in Fig. 6, a corresponding contribution to charging is estimated as $\Delta Q_{it} \sim 6x10^{10}$ q/cm^2 i.e., 20 times smaller than $1.2x10^{12}$ q/cm^2 of the total near interfacial oxide trap charging for 2MV/cm 1000 min stress in Fig. 5.

In the bias-temperature stress measurement, corona charge producing 2 MV/cm was deposited at room temperature on a selected wafer site. This wafer was placed on the hot chuck at the desired BTS temperature. After 5 min temperature stress, the wafer was cooled down and post-stress C-V was measured at the stressed site at room temperature.

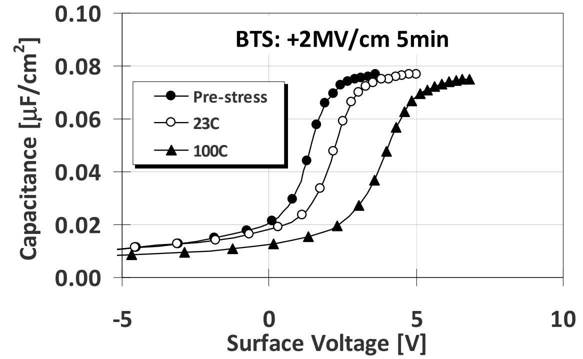

Fig. 7. Temperature effect on C-V instability. Curves for 23°C and 100°C stress are for different wafer sites.

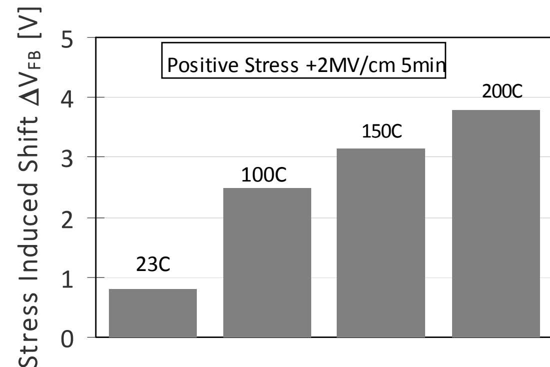

Fig. 8. The effect of temperature stress on the flatband shift measured at room temperature.

Enhancement of the oxide trap charging by increasing stress temperature is seen in Fig. 7. An increase of temperature from 23°C to 100°C increases the flatband shift from 0.9 V to 2.5 V. Results of further increasing of stress temperature are shown in Fig. 8. The bar graph in Fig. 8 presents results up to 200°C showing ΔV_{FB} increase to 3.8 V. To evaluate the thermal activation of oxide trap charging, the "time to failure", TTF, was introduced in Ref. 1. It is defined as stress time to reach a given high value of voltage shift. Based on the present results, TTF to the reach 2.5 V at 2 MV/cm bias stress decreased about 200 times from 1000 min at 23°C to 5 min at 100°C. This gives an estimated activation energy of about 0.6 eV for one way BTS compared to 1.1 eV reported for two-way BTS results for SiC MOSFETs [1].

A unique feature in the present approach is a means for distinguishing between BTS induced oxide trap charging and the effect of mobile ion drift. Both of these processes are illustrated in Fig. 9. An example related to sodium ion drift is given in Fig. 10. It compares a reference and sodium contaminated site. The latter is produced by touching the wafer. Whole wafer corona charging at created 1 MV/cm stress and the surface voltage was measured while the temperature was ramped with a rate of 5°C/min. Up to 150°C, the surface voltage increase is similar on the reference and contaminated sites. This indicates the bias-temperature stress negative charging of near-interface oxide traps. Above 150°C, the voltage decrease in the contaminated site takes place due to sodium ion drift to the SiC/SiO_2 interface. In Fig. 10, the Na contamination pattern is visible in the surface voltage map obtained with Kelvin force probe microscopy after BTS.

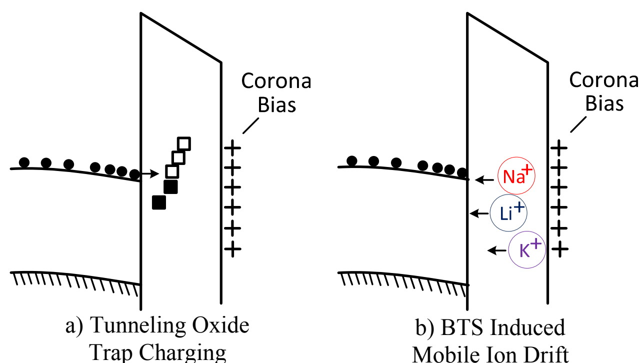

Fig. 9. Schematic of (a) BTS induced oxide trap charging and (b) mobile ion drift processes in oxidized SiC.

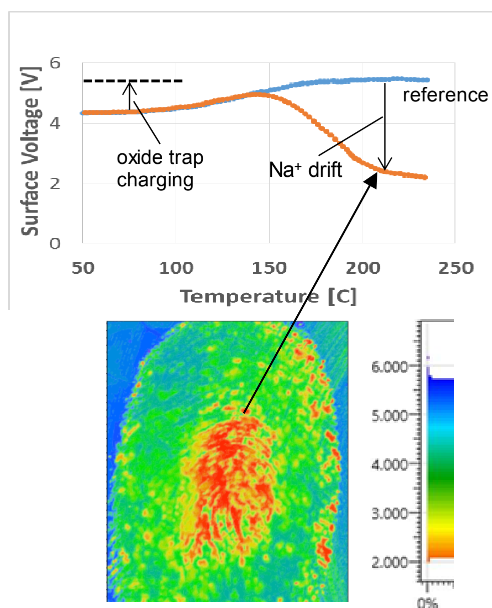

Fig. 10. Surface voltage vs. temperature for corona charge bias stress. Oxide trap charging increases V, whereas Na^+ drift decreases V. Map shows fingerprint Na contamination pattern.

Conclusion

We have demonstrated effective characterization of the interfacial instability in oxidized SiC achieved with the corona-Kelvin technique that does not require fabrication of any devices. The approach is validated by the results consistent with previous MOS and MOSFET measurements and with previous theoretical treatments of tunneling oxide trap charging. We have also demonstrated the possibility of monitoring of oxide trap charging instability and the mobile ion drift instability using surface voltage response to corona charge bias-temperature stress. This approach can be beneficial for whole wafer instability mapping leading to identification of localized weak instability regions.

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