Reduction of Metal Defect Formation through Process Optimization

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Introduction

Defects in the metal layers of capacitors cause HBT device failures [1]. The degree of capacitor breakdown can be characterized by the size and amount of deformities present. Optimization of the entire film stack reduces the effect of metal defects on devices [2]. This study focuses on irregularities in gold films and at gold platinum interfaces. Substrate structure, temperature, chamber pressure, and metal deposition rate play an important role in the construction of evaporated metal films [3]. These process parameters can be optimized to create uniform metal films in the capacitor layers of HBT devices. In this paper, we provide information on how to investigate and hone these factors to reduce defect formation in high volume manufacturing.

Process Conditions

An onsite reliability test showed that the bottom plate capacitor film stack was the most sensitive metal layer to defects that cause device failures. The bottom plate metal stack consists of 60 nm of titanium, 50 nm of platinum, and 1 µm of gold. This study is focused on Au and Pt films evaporated with an electron beam deposition system. Defects formed primarily due to the structure and substrate interactions of these films. Some metal films were deposited with a sputter deposition system for comparison. Substrate type, chamber temperature, chamber pressure, and deposition rate were varied for analysis. The Au e-beam source material was evaporated from a tungsten crucible. Pt e-beam material was evaporated from slug form.

Particle monitors are processed with each batch of product wafers to monitor defect formation. Single film monitor wafers are also included in this study. SiO substrates were prepared in a wet oxidation furnace. SiN and a-Si substrates were prepared in a plasma-enhanced CVD deposition tool. Some Si surfaces were treated using a solution of hydrofluoric acid and deionized water. The majority are untreated unless otherwise stated. Resistance measurements were taken with a four point probe. Stress measurements were taken by measuring changes in wafer bowing.

Defect Formation in Pt and Au Films

Deposited metal will be denser near substrate lattice dislocations [3]. Dense regions turn into defects with additional deposition (Figure 1). For this decoration to occur the substrate needs to be far enough from the source to be line of sight material growth. Deposition rate, chamber pressure, and substrate temperature also play an important role in metal-on-metal depositions. These parameters affect film stress and grain size. For metal layers to come together with a uniform interface which will not result in defects, the Pt and Au film structure must be optimized.

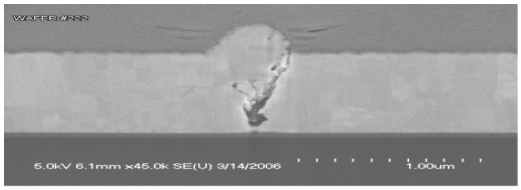

Fig. 1. Hillock formed at the Pt/Au interface.

Ripening defects were also observed in sputter deposited Au films with small grains (Figure 2). Grains at the surface of the films are not restricted from growth. The grains can grow at the surface it reduces total surface energy [4]. Ripening defects were also found on Pt/Ti film stacks on SiO (Figure 3). These defects form within the first fifteen minutes the wafers are at atmosphere. They do not occur on in the same films deposited on SiN.

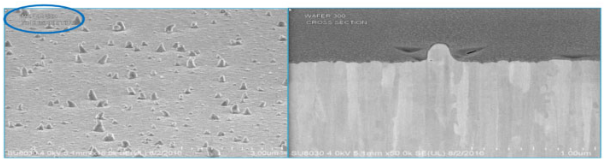

Fig. 2. Ripening defects in sputter deposited Au films.

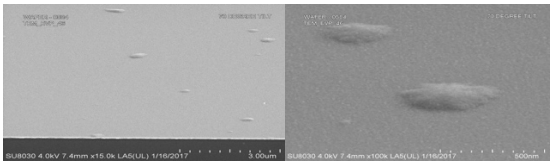

Fig. 3. Ripening defects in evaporated Pt/Ti films on SiO.

We found that 1um Au e-beam evaporated films on bare Si had fewer defects than the same Au films on e-beam evaporated Pt (Figure 4). Allowing Si wafers with Pt on them to sit at atmosphere for forty-eight hours before depositing Au resulted in reduced defect formation by a factor of ten. This is, in part, due to the relaxation of Pt films which can be measured though changes in film stress and sheet resistance occurring at room temperature.

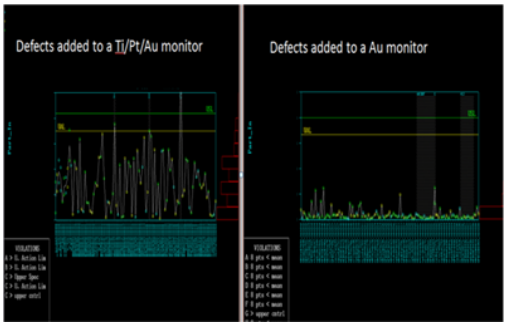

Fig. 4. Defects added by a Ti/Pt/Au film stack on Si (left) and defects added by a Au film on Si (right).

On bare Si, increasing the Au deposition rate by over 30% decreased the baseline defect count by more than 50%. On Si with a Pt layer on it, increasing the Au deposition rate by the same amount increased baseline defect counts by a factor of ten (Figure 5). However, an in situ Au growth pause of ten minutes between Pt and Au depositions at the same higher deposition Au rate reduced defect counts by half. This was still five times higher than the lower deposition rate Au on Pt. We found that targeting the Au rate to be double that of the Pt rate and allowing sufficient time between steps to allow the Pt to relax reduced overall defect formation in our process.

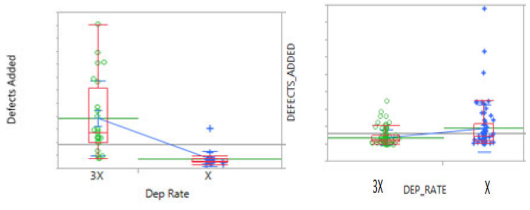

Fig. 5. Defect count as a function of deposition rate (Left) Effect of increasing the Au deposition rate on Pt; (Right) Effect of increasing the Au deposition rate on Si.

DATA COLLECTION TO REDUCE DEFECT FORMATION

Ostwald ripening effects are not uncommon in metal depositions [5]. Routine Ostwald ripening effects were observed in Au and Pt films in this study. Wilhelm Ostwald first discovered ripening effects in 1896 and they have been extensively modeled since [6]. Ripening effects have also been widely studied for their application in Au nanoparticle formation [7,8]. Changes in film structure can occur when there are two or more energy states of material. The energy state differential can be as simple as varying grain sizes. Larger grains absorb smaller grains to reduce total surface energy. The reaction will start to occur at room temperature in Pt and Au. The degree to which this occurs depends upon the free energy of the system. Ripening effects were encountered in this study and targeted for minimization.

Stress and sheet resistance data were collected on single film monitors to improve e-beam evaporated Pt and Au interfaces and overall film structure with ripening effects in mind. This data was collected to determine structural information about the films and their interaction with different substrate types. We found that substrate influence dictates alterations in Au stress and sheet resistance values at a thickness of 200 nm. Variations in film stress and resistance due to changes in film properties, such as grain size, were not observed until a micron of Au was tested.

Sputter deposited 200 nm Au films on Si have sheet resistance changes in the opposite direction as e-beam evaporated films of the same thickness and substrates. The e-beam films deposited on a-Si substrates change in a similar way to sputter deposited Au films (Figure 6). Careful selection of monitor wafers and film thickness is essential when characterizing alterations in film properties. Depending on the monitor wafer, the maximum RS change of evaporated 200 nm Au films was a decrease of 10.5% or increase of 21.5% over time until equilibrium was reached at room temperature. For the same films, the stress changed upwards of 250%.

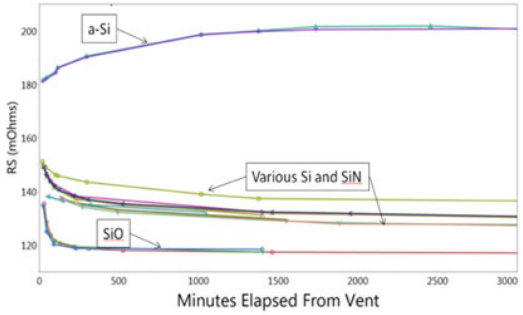

Fig. 6. 200 nm RS changes over time on different monitor wafers that were batched together when deposited.

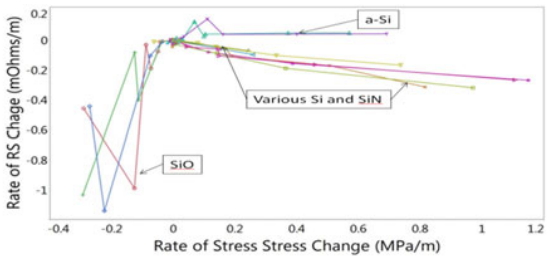

Fig. 7. Rate of RS change plotted by rate of stress change for different monitor wafers.

Treating the surface of bare Si wafers impacts the behavior of 200nm Au evaporated films. Six prime Si monitors were allowed to sit at atmosphere for nine days. Pure Si resistance decreases at atmosphere. We determined that they were fully saturated once the resistance stopped decreasing. Two wafers were treated with a 10:1 ratio of DI water to HF. Two more wafers were dipped in a 1600:1 ratio of DI water to HF. The other two wafers were left untreated. All six wafers were batched together and 200 nm of Au was deposited onto them with an e-beam tool. The resistance of 10:1 treated wafers increased by 2.7% and the stress increased by 170.1%. The resistance of 1600:1 treated wafers decreased by 7.3% and the stress increased by 110.3%. The resistance of the final two untreated wafers decreased 11.1%. The stress of these wafers increased 102.4%. After deposition the stress of all of the wafers was compressive however over time they turned tensile. The stress crossed zero in the first three hours (Figure 8). All of the films came to equilibrium after three days.

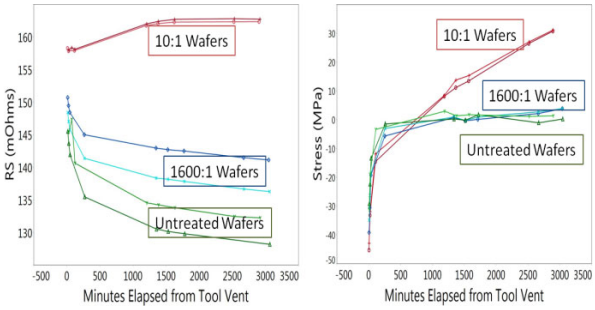

Fig. 8. Changes in e-beam evaporated film properties with Si surface treatment.

We observed that changing the crystal orientation of the Si also changed the results. (100) Si was used in the experiment described in the above paragraph. We also tested (111) Si. The resistance of the same 200 nm evaporated Au decreased 17% and the stress increased 80%. When Au was deposited on Si with varying different crystal orientations and surface compositions, the resistance and stress evolved in differing manners. The free energy of the system differentially affects the stress or resistance depending on the avenue of greatest potential energy decrease.

We chose, 200 nm Au and 20 nm Pt, metal thicknesses for this study, in part, due to the sensitivity of their resistance response. Resistance data collected from a film that is thinner than the mean free path of an electron in a material provides information that is more sensitive to film thickness and structure than data collection from a thicker film. This is due to the infinitely thick thin film (ITTF) limit [9,10]. The ITTF limit occurs when the film is thick enough to allow free electron flow. The resistivity will still not match bulk values due to differences in the way bulk material and thin films are manufactured. Below the ITTF limit, small changes in thickness, grain structure, and surface roughness can easily be measured through resistance. The influence of the substrate and film ripening at room temperature renders this technique troublesome. The use of an additional material layer to reduce the free energy of the system creates repeatable, reliable information about the metal film. With a supplemental layer, the change of Au film RS declined to less than 1% and stress change diminished to 4% before reaching equilibrium.

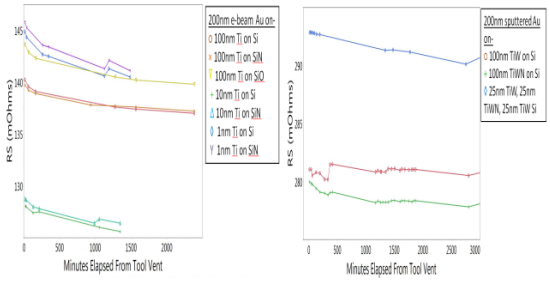

Fig. 9. (Left) Change in RS of e-beam films; (Right) Change in RS of sputtered films.

RS changes of 20 nm e-beam evaporated Pt films on SiO were measured. They decrease over time at room temperature (Figure 10). 4.5 nm Pt films were also tested in with a 35 nm Ti layer on top. When deposited on SiN this film stack is sensitive to SiN substrate thickness. To show this, film RS was tested once equalibrium was reached on a skew of SiN thicknesses (Figure 10). We found that the metal stack RS was less sensitive to SiO substrates. When the same metal film stack was deposited on SiO and SiN it was found that the metal RS was more repeatable on SiO but the defects were much worse. After fifteen minutes at atmosphere the metal stack on the SiO would max out the defect measurement tool. Further investigation showed the appearance of the defects in Figure 3.

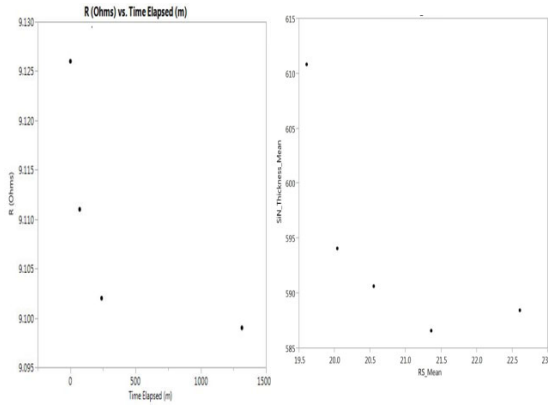

Fig. 10. (Left) 20nm Pt on SiO RS relaxation over time; (Right) 4.5 nm Pt with 35 nm Ti on top RS mean vs SiN thickness.

CONCLUSION

Irregularities in Au films and at Au Pt interfaces are dictated by film structure and interactions with the substrate. Process parameters influence the metal film construction and interactions. The arduous and careful study of these films resulted in process optimization. Tuning the process reduced defects which improves HBT device reliability. Through this study, we found that having a Au deposition rate twice the Pt rate was optimal for our bottom plate capacitor metal stack. It is important to give the evaporated material enough time and energy to smooth out any lattice dislocations but not so much energy that it will decorate subtle imperfections in the substrate it is being deposited on. The addition of a supplemental layer between the substrate and metal film may also be utilized to understand film structure and reduce interface reactions.

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REFERENCES

[1] Ueda O., Pearton S. (2013.) *Materials and Reliability Handbook for Semiconductor Optical and Electron Devices*, New York (NY): Springer-Verlag.

[2] Rao M., O'Niel S., Tiku S. (2003). *Metal Particle Effects on Thin Film Capacitors in High Volume Manufacturing*. Paper presented at 2003 International Conference on Compound Semiconductor Mfg

[3] Ohring M., (2002) *Materials Science of Thin Films, Deposition and Structure*, San Diego (CA): Academic Press.

[4] Wong C.C, Smith H.I, Thompson C.V. (1985). *Surface-energy-driven Secondary Grain Growth in Thin Au Films*. Appl. Phys. Lett. Volume 48. Issue 5.

[5] Ratke L., Voorhees P. W. (2002). *Growth and Coarsening, Ripening in Material Processing*, Berlin Heidelberg, New York: Springer-Verlag,

[6] Baldan A. (2002). *Review of the Progress in Ostwald Ripening Theories and Their Applications to Nickel-Base Superalloys Part I: Ostwald Ripening Theories,* Journal of Materials Science. Volume 37. Issue 11.

[7] Ruffino F., Grimaldi M. G., Giannazzo F., Roccaforte F., Raineri V., Bongiorno C., Spinella C. (2009). *Kinetic Mechanisms of the in situ Electron-Beam Induced Self-Organization of Gold Nanoclusters in $Si0_2$*, J. Phys. D: Appl. Phys. 42

[8] Hannon J. B., Kodambaka S., Ross F. M., Tromp R. M. (2006). *The Influence of the Surface Migration of Gold on the growth of Silicon Nanowires*, Nature 440.

[9] Tellier C.R. (1978). *A Theoretical Description of Grain Boundary Electron Scattering by an Effective Mean Free Path, Thin Solid Films*. Volume 51. Issue 3.

[10] Angadi M.A., Udachan L.A. (1981). *The Effect of the Deposition Rate on the Electrical Resistivity of Thin Tin Films,* Thin Solid Films. Volume 78. Issue 3.

ACRYONYMS

HBT: Heterojunction Bipolar Transistor
HF: Hydrofluoric Acid
DI: Deionized
ITTF: Infinitely Thick Thin Film