Iridium Plug Technology for AlGaN/GaN HEMT Short-Gate Fabrication

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Keywords: GaN HEMT, embedded gate technology, sputtered Ir, Au diffusion

Abstract

The purpose of this work is to introduce a novel concept for the AlGaN/GaN HEMT embedded gate fabrication. The novelty of the proposed gate fabrication method is to obtain a stress relief volume inside short embedded gates (150 nm and less). This volume compensates strain generated during device processing after gate module definition or during device operation. The presented technology was used for the fabrication of the mockup gates on GaAs substrates in order to confirm that the desired geometrical shape can be obtained. The mechanical simulation of conventional embedded gates and embedded gates with strain relief volume showed the effect of stress reduction during wafer cooling down to room temperature after transistor passivation process.

INTRODUCTION

The embedded gate technology where the gate is defined by a trench in a pre-existing passivation layer is quite widespread and commonly used in the technological process of AlGaN/GaN HEMT fabrication. As reported in [1] embedded gate technology facilitates the application of a metal sputter process for Schottky gate fabrication which has technological advantages and leads to higher device stability and reliability. In this work, a further evolution of the "sputtered Ir" approach intended for short gate fabrication is presented. As the design of the short gates has to be optimized for minimum parasitic gate cap capacitance, the use of tall gates and consequently high aspect ratio gate trenches is preferable. The presented technology combines high aspect ratio gate trench etching with thick Ir film deposition. Ir deposition is optimized such that the coalescence of the Ir film edges occurs at the top of the gate trench. Therefore an Ir plug is formed with a tiny cavity alongside of the gate in the center. This structure combines conformal coating of the gate trench with a mechanically flexible gate construction (due to the cavity) which largely reduces mechanical strain build up in the gate region. This is in contrast to gate trench technologies employing a complete filling of the trench with Au. The new technology thus prevents the appearance of high mechanical stress and consequently mechanical damage of the structure. Furthermore, Au diffusion from the gate to the semiconductor surface [2, 3] is one of the reported degradation mechanisms. It was shown that Au diffused towards the Schottky interface is responsible for the increase of the drain and gate leakage current during high temperature operation test. Conventional gate fabrication technology based on the electron-beam evaporation of the gate metal has often been used. E-beam evaporation of the gate metal in combination with the gate trench often causes cracks and voids in the Schottky metal film especially in the trench corners and trench sidewalls. These voids and cracks allow Au to diffuse towards the semiconductor surface along the SiNx/Schottky metal interface. In contrast to evaporated gate metallization Ir sputter technology provides both, a very efficient diffusion barrier against gold and a widely conformal coating of the gate trench. Thus cracks in the metal and voids at the gate metal / trench interface are effectively avoided. The introduction of slanted gate trench sidewalls and sputtered Schottky metal further improves the

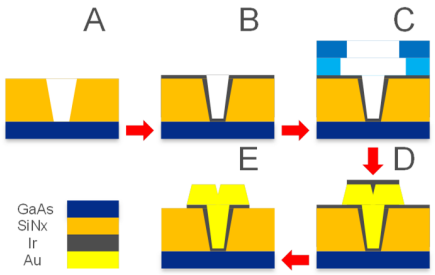

Fig. 1. Sputtered Ir gate fabrication process flow.

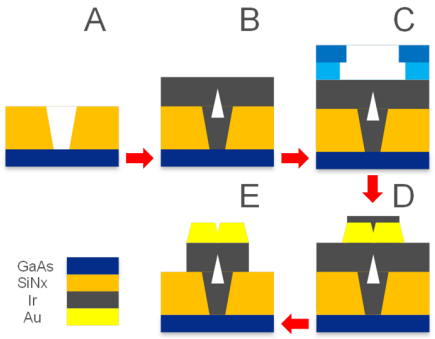

Fig. 2. Ir-plug gate fabrication process flow.

situation (Fig. 1). Nevertheless, due to the roughness of the gate trench sidewalls and mechanical strain generated by thermal expansion of the gate metal cracks and voids may arise in the Schottky metal during the further processing or transistor operation. As the Au/semiconductor surface separation is defined by the thickness of the Schottky metal any holes or cracks appearing due to these reasons will provide a path for Au diffusion towards the semiconductor surface. In order to completely avoid this situation, the "Ir-plug" gate technology shown in the Fig. 2 has been developed. Using this technology the distance between Au and semiconductor surface is defined by the sum of the Schottky metal thickness and the thickness of the passivation layer and can be up to 10 times higher as compared to conventional technology. Another important feature of the "Ir-plug" technology is the strain relief volume formed in the gate body. This may accommodate any strain that appears due to mismatch of thermal expansion coefficients of the materials used in the gate module (Table 1). As can be seen from the Table 1, Au has the largest linear thermal expansion coefficient among all the materials used. Thus the presence of Au in the gate trench can cause cracks and voids due to the thermal expansion mismatch for example during production steps following wafer processing such as for example soldering at temperatures of typically 350°C.

TABLE I
PHYSICAL PROPERTIES OF THE MATERIALS
USED IN THE GATE FABRICATION PROCESS

Material	**Linear Thermal Expansion Coefficient (10^{-6}×m/(m×K))**	**Young's Modulus (GPa)**	**Poisson Ratio**
AlGaN	≈5.5	N/A	N/A
Ir	6.4	528	0.26
Au	14.2	78	0.44
SiN_x	3.3	300	0.27

EXPERIMENT

For developing of "Ir-plug" technology, mockup gates were fabricated on 4 inch n-type GaAs wafers. The ohmic contact metal stack relies on a Ti/Al based metallization. It was deposited in order to emulate the source contact topology. A 300 nm thick SiN_x film was deposited using PECVD. ZEP resist was used for the gate trench etch mask formation with subsequent thermal reflow and highly anisotropic ICP-etching in order to obtain sloped gate trench sidewalls. Immediately after gate trench etching the wafers were coated with a 300 nm thick Ir film using DC magnetron sputtering. Afterwards a two layer PMMA mask has been applied for lift-off deposition of the gate head metal. It consisted of electron-beam evaporated Ti/Au/Ir gate metal stack. A sacrificial Ir layer (evaporated) has then been deposited on top of the gate head metal stack in order to facilitate self-aligned back-etching of the sputtered Ir layer. At the last step wafers were etched in Cl_2/O_2/He ICP plasma using gate metal as an etch mask for Ir film removal.

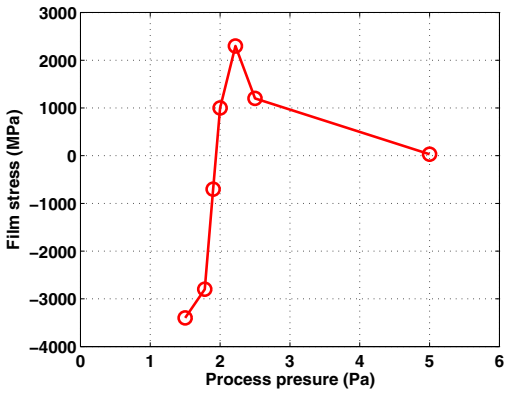

Fig. 3. Dependence of the Ir film stress on the sputtering process pressure (negative stress = compressive, positive stress = tensile).

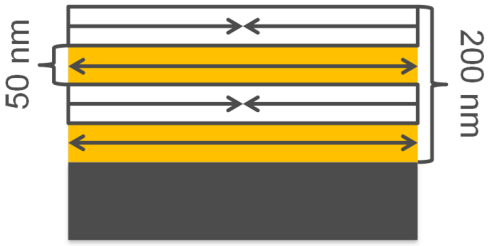

Fig. 4. Strain compensation layer sequence for the thick Ir film deposition.

MOCKUP GATE FABRICATION RESULTS

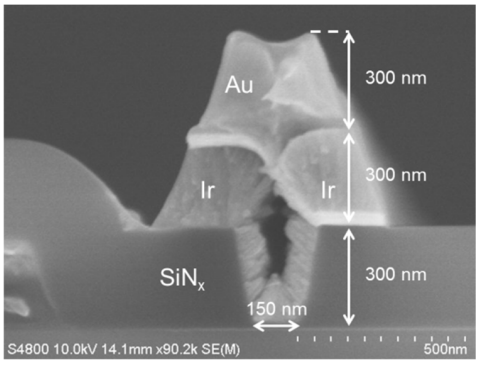

Fig. 5. Cross-section of the Ir-plug gate mockup.

Fig. 2 shows that an Ir film thickness comparable to the gate trench depth has to be used in order to obtain film coalescence at the top of the gate trench. The deposition of thick Ir films is typically accompanied by strong internal mechanical strain leading to film delamination from the substrate. This can be avoided by controlling Ir film stress using alternating sputtering conditions during thick Ir deposition. Deposition of Ir at suitable stress conditions depends on the pressure during the sputtering process (Fig. 3). The strong change of the film strain in a very narrow pressure range hardly allows sputtering of films with zero strain. In order to overcome this problem, an alternative approach with deposition of 4 layers with oppositely directed strain of the same magnitude was used (Fig. 4). In this approach the full film thickness is divided in four equal parts and the sputtering process performed in four steps with different pressure. This approach allows for compensation of any pressure instability and thick Ir films (up to 300 nm) with total internal strain close to zero could be obtained. Fig. 5 shows the cross-section of the mockup gate fabricated. It can be seen, that gate trench coverage is conformal, and the Ir film coalesces at the top of the gate trench. No Au penetration inside the Ir plug is observed. The next step of

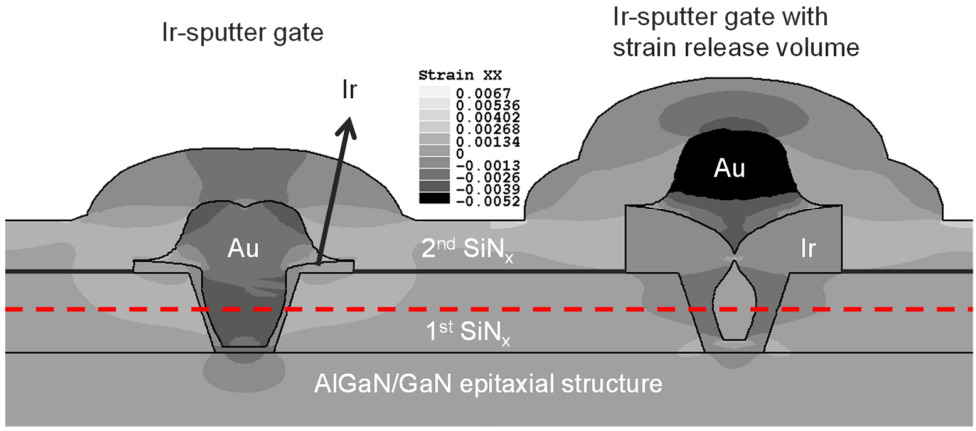

Fig. 6. Simulated strain distribution in conventional Ir sputter gate (left) and Ir sputter gate with strain relief volume (right).

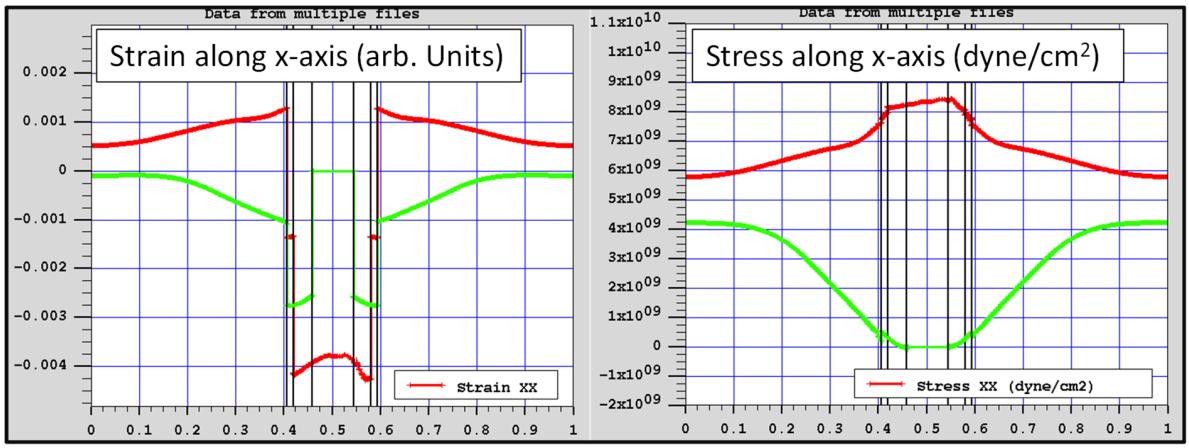

Fig. 7. Simulated stress and strain distribution along the cutline showed in Fig. 6 for conventional Ir sputter gate (red lines) and Ir sputter gate with strain relief volume (green lines).

the development is implementing the new gate in the technological process of AlGaN/GaN HEMT fabrication and a subsequent verification of the electrical performance and reliability of the new transistors.

Simulation of Stress and Strain Inside the Structure

In order to confirm stress relief properties of the void inside the gate, Silvaco© Victory Stress© software was used, and the following simulation was performed: The two structures used in the simulation are shown in Fig. 6. Conventional Ir-sputter gate (Fig. 6 left) has a 100 nm thick Ir layer and a gate trench filled with Au. Ir-sputter gate with strain relief volume has a 300 nm thick Ir film that coalesces in the upper part of the trench and does not allow Au penetration inside the trench. Therefore the void is formed inside the gate body. The physical properties of the materials, which were used in the simulation, are given in the Table 1.The boundary conditions were set in such a way that lateral edges of the simulation domain were fixed and free movement was only allowed in Y direction (up). In order to simulate the effect of mechanical stress appearing due to the deposition of the second SiN_x film the whole structure was assumed to be in equilibrium at 350 °C (after deposition of SiN_x film) initially and then cooled down to room temperature. The mechanical stress appearing due to the difference in thermal expansion coefficients of different materials was calculated. Knowledge of mechanical stress, Young's modulus and Poisson ratio of all materials in the structure allows calculation of the strain appearing in different materials. Fig. 6 shows the results of this calculation. As can be seen from Fig. 6 (left), a significant shrinkage occurs during cooling process (0.4%) in the conventional structure where the gate body is filled with Au. The consequence of Au and SiN_x shrinkage is the build-up of tensile stress (up to 800 MPa) inside the gate and next to the trench edges (Fig. 7 right red lines). The value of this stress is much more than the built-in stress of the SiN_x film itself (≈500 MPa); the potential problem is the presence of two interfaces (Au/Ir and Ir/SiN_x) where materials are torn apart from each other. In this situation, delamination of Ir from SiN_x or from Au can occur. The consequence of such delamination is formation of cracks and voids that can provide a migration path for Au towards AlGaN surface. Fig. 6 (right) shows the situation that takes place in the Ir-plug gate. As can be seen from the figure no shrinkage occurs in the void inside the gate body. This prevents stress formation: zero stress inside the gate void and less than 10 MPa stress at the interfaces can be seen (Fig. 7 right green lines).

Conclusions

A novel approach for AlGaN/GaN HEMT embedded gate fabrication was developed. As compared to conventional embedded gate technology, where Au completely fills gate trench, in the proposed concept the gate body is empty. The void inside the gate acts as a stress relief volume. Mockup gates were fabricated on GaAs substrates in order to prove the desired geometrical shape of the gate. Consequent simulation of the transistor's passivation process, which includes deposition of the SiN_x film at high temperature, showed the expected functionality of the stress relief volume and a significant reduction of the stress building up on the Ir/SiN_x interface.

Acknowledgements

The authors would like to thank the team of the microwave department for the transistor measurements. Additionally, the support from the process technology department is appreciated. This work was supported by the "GaNSaT" project (EC – Contract nº 606981) in the 7th Framework Program Research. Authors also acknowledge Dr. Bahat-Treidel for help with the strain simulation.

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Acronyms

HEMT: High Electron Mobility Transistor
ICP: Inductively Coupled Plasma
DC: Direct Current
PECVD: Plasma Enhanced Chemical Vapor Deposition
PMMA: Poly Methyl Meth Acrylate