

# High Aspect Ratio Vias in Silicon Carbide Etched by Inductively-Coupled Plasma

Marko J. Tadjer<sup>1</sup>, Lunet E. Luna<sup>2</sup>, Eugene A. Imhoff<sup>1</sup>, Travis J. Anderson<sup>1</sup>, Karl D. Hobart<sup>1</sup>, Fritz J. Kub<sup>1</sup>

<sup>1</sup>U.S. Naval Research Laboratory, 4555 Overlook Ave SW, Washington DC 20375, USA

<sup>2</sup>National Research Council, Washington DC, USA

**Keywords:** Silicon Carbide, inductively coupled plasma, etch, dry, aspect ratio, deep etching, Bosch etching

## Abstract

We report the development of a high aspect ratio inductively coupled plasma (ICP) etch process for 4H-SiC. Feature sizes as narrow as 2  $\mu\text{m}$  were etched at a rate of 0.18  $\mu\text{m}/\text{min}$ , with an etch rate as high as 0.43  $\mu\text{m}/\text{min}$  measured as feature size was increased to 10  $\mu\text{m}$ . Aspect ratios above 10 were routinely obtained using an electroplated Ni mask. Via shape was tapered at about 8° angle independent of substrate offcut angle using SF<sub>6</sub>/O<sub>2</sub> chemistry. Additional experiments were carried out in order to etch vias with nearly vertical sidewalls.

## INTRODUCTION

Over the past decade, the compound semiconductor industry has witnessed Silicon Carbide enter the mainstream market for power devices. One contributing factor to the success of this wide bandgap material has been the corresponding evolution in fabrication processes such as thermal oxidation and doping activation annealing, among others. Its wide bandgap, high thermal conductivity, and mechanical hardness have turned SiC into an attractive material choice for a number of applications, among which microelectromechanical systems (MEMS) and power switching devices. Thus, processing of vertical SiC structures has become an enabling technology, both from an electrical and a mechanical application standpoint. While commonplace for Si, reports of dry-etched deep vias in SiC have mostly focused on etching relatively low aspect ratio structures, although most recent reports of high aspect ratio SiC trenches have been quite encouraging [1-6]. In this paper, we report the development of a deep reactive ion etch (DRIE) process for SiC vias with aspect ratios of at least 12 achieved with a feature width of 2  $\mu\text{m}$ , and a maximum depth of 52  $\mu\text{m}$  using a 10  $\mu\text{m}$  feature width.

## EXPERIMENTAL DETAILS

The experiments were conducted using n<sup>+</sup>-doped 100 mm 4H-SiC substrates, obtained commercially. The etch mask process commenced by seeding the Si-face with a blanket layer of 10/100 nm Cr/Au metal stack, deposited by e-beam evaporation. Patterns of various length/width ratio in the 2-20  $\mu\text{m}$  range were patterned using photoresist (Shipley 1818). A Nickel film of at least 1.1  $\mu\text{m}$  thickness, to serve as a hard mask for the dry etch process, was then electroplated

on the patterned wafers using the Au seed as an adhesion layer. Following a solvent clean step to remove the photoresist and expose the remaining non-plated Au, a blanket ion mill step was performed in order to remove 110 nm of metal from the wafers, thus exposing the SiC surface in the non-plated features of the pattern.

Etching experiments were performed on either full wafers or diced coupons using an STS inductively-coupled plasma (ICP) etcher. Two etch chemistries were compared. The first process was based entirely on an SF<sub>6</sub>/O<sub>2</sub> plasma etch, whereas the second process involved a C<sub>4</sub>F<sub>8</sub>-based deposition step before the SF<sub>6</sub>-based etch (similar to a Bosch process in Si). Process temperature was controlled using a backing He pressure of 10 Torr, while the chamber sidewalls were kept near room temperature by a separate cooling circuit. Similarly to Si, both the etch rate and anisotropy were expected to be temperature sensitive for SiC DRIE [7]. To improve the electrothermal coupling to the platen, a conductive SiC carrier wafer and pump oil were used to mount the coupons [8].

The as-etched structures were cleaved along the c-axis and cross-sectional scanning electron microscopy was performed to evaluate etch rate by measuring the depth of the etched trenches. Additional characterization was performed using a KLA-Tencor step height measurement instrument as well as a KLA-Tencor MicroXAM optical profilometer, with a good agreement of the data.

## RESULTS AND DISCUSSION

To the extent possible, process conditions were kept consistent between the C<sub>4</sub>F<sub>8</sub>/O<sub>2</sub>-based etch and the SF<sub>6</sub>/O<sub>2</sub>-only etch, as shown in Table I. The etch rate for SiC has been reported to not be very sensitive to the O<sub>2</sub> percentage, thus we kept the O<sub>2</sub> flow rate constant at 5 sccm as well [9].

TABLE I.  
COMPARISON OF SF<sub>6</sub>/O<sub>2</sub> AND C<sub>4</sub>F<sub>8</sub>/O<sub>2</sub> BASED ETCH PROCESSES

Process Parameter	SF <sub>6</sub> /O <sub>2</sub> Etch	C <sub>4</sub> F <sub>8</sub> /O <sub>2</sub> Deposition	SF <sub>6</sub> /O <sub>2</sub> Etch
Pressure (mT)	5	5	5
Platen Temperature (°C)	~40	~40	~40
SF <sub>6</sub> (sccm)	50	-	50
O <sub>2</sub> (sccm)	5	5	5
C <sub>4</sub> F <sub>8</sub> (sccm)	-	50	-
ICP/RIE Power (W)	850/85	850/85	850/85
Cycle duration (s)	-	15	15
Etch Rate ( $\mu\text{m}/\text{min}$ )	~0.18-0.43		~0.21

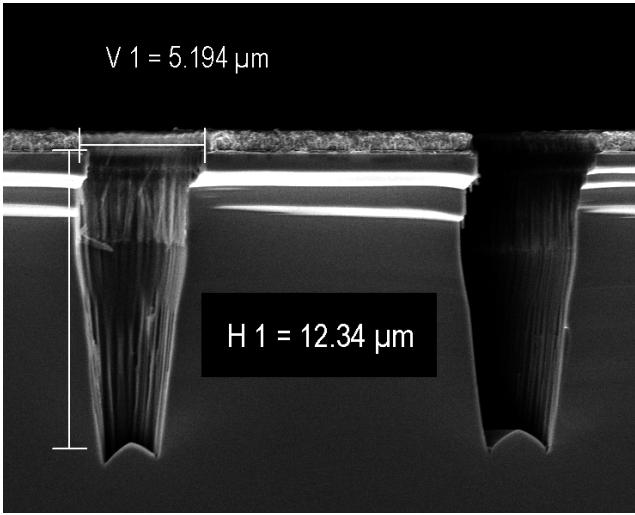


Fig. 1. Cross-sectional SEM image of SiC via sidewall profile etched using a 1 hour long (120 cycle) Bosch etch.

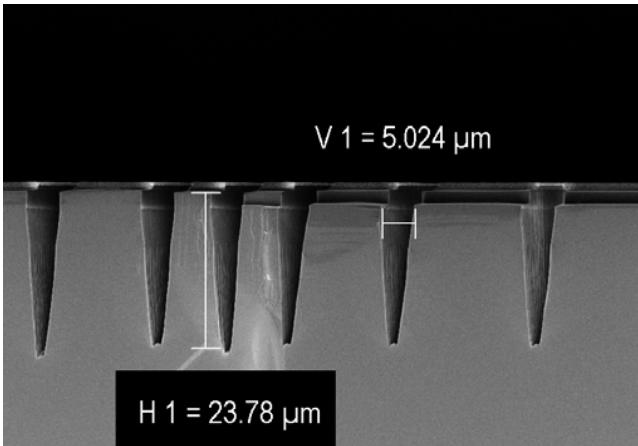


Fig. 2. Cross-sectional SEM image of a coupon-scale etch of 4H-SiC substrate using  $\text{SF}_6/\text{O}_2$  ICP process for 1 hour on a poly-SiC carrier wafer.

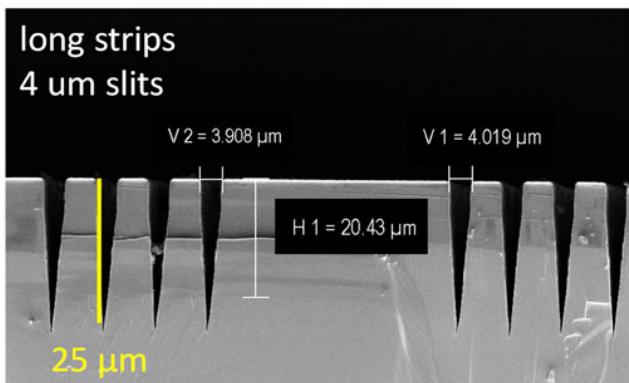


Fig. 3. Cross-sectional SEM image of a wafer-scale etch of 4H-SiC substrate using  $\text{SF}_6/\text{O}_2$  ICP process for 1 hour.

Figure 1 shows the etch profile of SiC vias etched using the  $\text{C}_4\text{F}_8$ -based Bosch-like process described in Table I. A corrugated sidewall profile was observed, much as is the case with a Si Bosch process where passivation and etch cycles alternate. A key difference was the slanted sidewall profile and the trenching observed in the bottom (i.e., W-shaped bottom) indicative of ion reflection towards the bottom instead of reacting at the SiC sidewall. This undesirable feature is possible to correct using an appropriate combination of process parameters (i.e., temperature, pressure, and DC bias). However, owing to the fact that SiC already has C incorporated into the lattice, we observed that the fluorocarbon-based passivation step may be possible to eliminate as long as there is sufficient Oxygen in the etch chemistry.

To test this hypothesis, we implemented an  $\text{SF}_6/\text{O}_2$  etch chemistry with typical conditions summarized in Table I. Figures 2 and 3 show SiC etch profiles obtained by this process on a coupon and wafer scale, respectively, after a 1 hour long process. The slightly lower etch rate obtained when the etch was performed on a coupon (Fig. 2) was likely due to chamber loading effects as the coupons were mounted on a polycrystalline SiC carrier wafer. The etch depths depicted in Fig. 2 and 3 were about twice as high as the one obtained from the Bosch process, indicating that the continuous  $\text{SF}_6/\text{O}_2$  chemistry had good sidewall selectivity and minimal unreacted ion propagation towards the trench bottom.

We thus proceeded to study the etch profiles upon longer etching times. Using the  $\sim 1 \mu\text{m}$  thick Ni hard mask, up to 4 hour long etch processes were developed. Figures 4-6 present the cross-sectional profiles upon a 2-hour long etch as a function of feature width (2, 5, and  $10 \mu\text{m}$ ). Apart from preserving the smooth sidewall profile and observing a dependence of etch depth on feature width, two other phenomena were observed when the trench width became 5  $\mu\text{m}$  or narrower. For the  $5 \mu\text{m}$  slit width in Fig. 5, a slightly-curved V-shaped bottom was observed instead of the W-shaped bottom caused by trenching in wider vias. This effect was even more visible in Fig. 6 ( $2 \mu\text{m}$  slit width), where the trench sidewalls were essentially vertical up to  $24 \mu\text{m}$  depth, followed by an irregularly-shaped V-like trench, which was likely due to insufficient ionized species evacuation at the 5 mT process pressure.

A set of experiments which varied pressure, power, temperature, and gas flow rates were designed in order to obtain fast, tapered etches on one end of the spectrum, as described in this paper, towards a slower, more vertical etch profile at the other end. Finally, we note that a more advanced process control was possible if a switched process incorporating alternating steps with different conditions is implemented, where one step is optimized for sidewall etching and the other one preferentially etched the via bottom in order to yield a combined trench profile with vertical sidewalls. This is the subject of our future process development effort [10].

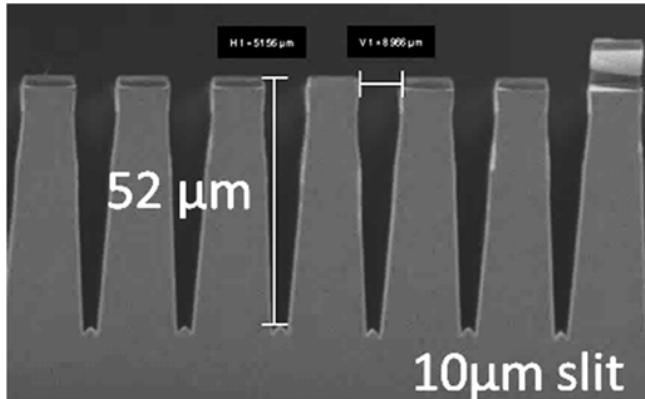


Fig. 4. Dependence of etch depth on ratio of length to width of opening in the Ni mask (coupon etch, 2 hrs, 10  $\mu\text{m}$  via opening).

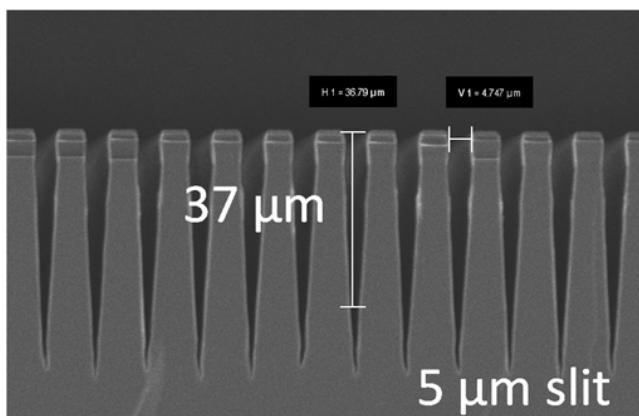


Fig. 5. Dependence of etch depth on ratio of length to width of opening in the Ni mask (coupon etch, 2 hrs, 5  $\mu\text{m}$  via opening).

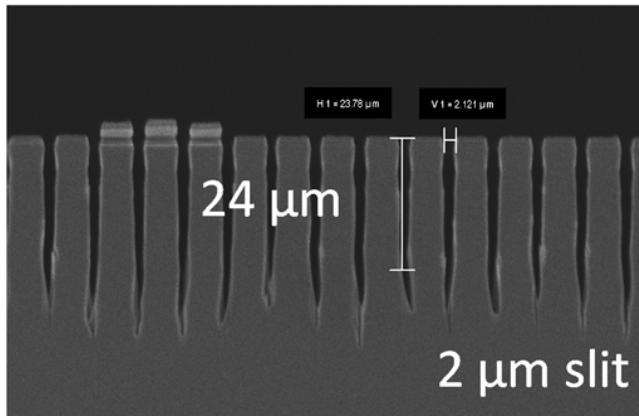


Fig. 6. Dependence of etch depth on ratio of length to width of opening in the Ni mask (coupon etch, 2 hrs, 2  $\mu\text{m}$  via opening).

## CONCLUSIONS

A high aspect ratio ICP etch of deep vias in 4H-SiC was demonstrated with feature size as narrow as ~2  $\mu\text{m}$  and depth of up to about 52  $\mu\text{m}$ . The etch process exhibited good selectivity to the electroplated Ni mask (>50:1), a highly

anisotropic etch profile, and a relatively fast etch rate. Combined, these features enabled the demonstration of a high aspect ratio process for deep SiC vias, a necessary step for advanced SiC-based MEMS and power devices.

## ACKNOWLEDGEMENTS

The authors acknowledge Mr. Milton Rebbert, Mr. Neil Green, Dr. Konrad Bussman, Mr. Walter Spratt, and Mr. Dean St. Amand for NRL processing equipment support and sample preparation. Research at NRL was supported by the Office of Naval Research. L.E.L. gratefully acknowledges postdoctoral support from the National Research Council.

## REFERENCES

- [1] Z. Ring, "Method of forming vias in silicon carbide and resulting devices and circuits," US Patent # 6,475,889, November 5, 2002.
- [2] P. Chabert, "Deep etching of silicon carbide for micromachining applications: Etch rates and etch mechanisms," J. Vac. Sci. Technol. B 19, 1339 (2001).
- [3] S. Tanaka, K. Rajanna, T. Abe, and M. Esashi, "Deep reactive ion etching of silicon carbide," J. Vac. Sci. Technol. B 19, 2173 (2001).
- [4] C. Han, Y. Zhang, Q. Song, Y. Zhang, X. Tang, F. Yang, and Y. Niu, "An Improved ICP Etching for Mesa-Terminated 4H-SiC p-i-n Diodes," IEEE Trans. Electr. Dev., vol. 62, no. 4, pp. 1223, 2015.
- [5] L.J. Evans and G.M. Beheim, "Deep Reactive Ion Etching (DRIE) of High Aspect Ratio SiC Microstructures using a Time-Multiplexed Etch-Passivate Process," Mater. Sci. Forum, vols. 527-529, pp. 1115-1118, 2006.
- [6] K.M. Dowling, E.H. Ransom, and D.G. Senesky, "Profile Evolution of High Aspect Ratio Silicon Carbide Trenches by Inductive Coupled Plasma Etching," J. of Microelectromechanical Systems, vol. 26, no. 1, pp. 135-142, 2017.
- [7] S. Aachboun and P. Ranson, "Deep Anisotropic Etching of Silicon," J. Vac. Sci. Technol. A, vol. 17, no. 4, pp. 2270, 1999.
- [8] L.E. Luna, M.J. Tadjer, E.A. Imhoff, T.J. Anderson, K.D. Hobart, F.J. Kub, "Dry etching of high aspect ratio 4H-SiC microstructures," ECS Jour. Solid State Sci. Technol. 6 (4) P207-P210 (2017).
- [9] P.H. Yih, V. Saxena, and A.J. Steckl, "A Review of SiC Reactive Ion Etching in Fluorinated Plasmas," Phys. Stat. Sol. (b) 202, 605, 1997.
- [10] L.E. Luna, M.J. Tadjer, T.J. Anderson, E.A. Imhoff, K.D. Hobart, and F.J. Kub, "Deep reactive ion etching of 4H-SiC via cyclic SF<sub>6</sub>/O<sub>2</sub> segments," under review.

