Plasma Dicing on Tape for GaAs Based Devices

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Abstract

Gallium-based III-V semiconductors such as GaAs are widely used in light-emitting diode (LED), wireless, and laser diode devices. Thin GaAs devices have increased performance compared to full-thickness ones, but the challenge remains to separate the thin die without damaging the device. A novel dicing process based on plasma, defined as "Plasma Dicing on Tape" (PDOT), can overcome the limitations of conventional methods like saw, scribe and break, and laser for thin GaAs devices, as has been already demonstrated for silicon-based devices. Plasma dicing technology also has the possibility to reduce production costs by reducing the street widths between die, thereby increasing the number of die on each wafer.

INTRODUCTION

Gallium-based III-V semiconductors such as GaAs are widely used for transistors including MESFET, HEMT, HBT, optical emitters such as laser diodes, photodetectors, and solar cells (typically multi-junction). In many cases the thermal and electrical performance of GaAs devices can be improved by designing and fabricating devices on thinner substrates [1]. Practically, however, thinned GaAs wafers pose a yield challenge during device manufacturing — particularly for the backside processing and packaging operations. The economics of potential device performance improvement for thinner substrates must be weighed against the yield loss impact during fabrication.

During the thinning operation, the full-thickness GaAs substrates are typically mounted to a rigid carrier and thinned using a grinding process in conjunction with a combination of polishing and/or chemical etching. The current state of the art thins 3" to 6" wafers with starting thicknesses up to 675 µm down to 75-100 µm, with more advanced designs using wafer thicknesses of 60 µm and below. [4]

Once the wafer has been thinned, backside wafer processing is performed — including the formation of through-wafer vias and subsequent backside metallization. Once device fabrication is complete, the next challenge is to separate the die at the end of the process while maintaining high throughput and dicing yield.

Most current techniques used to separate GaAs die are based on mechanical methods. Initially, saw dicing was the predominant dicing technique, but limitations such as kerf widths greater than 40 µm, and the slow feed speeds required to avoid cracks and damage to the devices, resulted in a high cost of ownership [4]. The scribe-and-break technique avoids many of the problems associated with sawing. In this technique, a stylus is used to scribe lines along a crystal axis on the wafer with carefully controlled speed and angle. The breaking operation is accomplished by flexing the wafer using a roller and anvil. Scribe and break is faster than saw dicing but it can be a very delicate process, especially for small die. Scribe and break is effective only along crystal axes within the substrate, which requires careful alignment of device layout on the substrate. The scribe-and-break operation can still induce damage to the die due to chipping, bruising and alignment problems [4].

Laser dicing today represents the most used technique to separate die, especially for very thin wafers, because it guarantees low chipping and cracks with a kerf width of 30 µm. The main disadvantage of this technique is that it requires an additional protective layer on the die to contain recast slag. Even if chipping and cracking is lower compared to saw dicing or scribe and break, slags present on the sidewalls and heat affected zones can still create stress and damage to the device. A way to reduce the slags is to use a critical laser intensity that vaporize the material. In order to optimize the quality of the cut, multiple laser passes are usually utilized instead of a high-power single cut, increasing significantly the dicing process time [4].

A novel dicing process based on plasma, defined as "Plasma Dicing on Tape" (PDOT), can overcome the limitations of both mechanical and laser dicing, as already demonstrated for silicon-based devices [5]. In plasma dicing, an etch mask, such as photoresist (PR), protects the die while high-energy plasma formed from specific gases, such as $SiCl_4$, BCl_3, and Cl_2, etches through the exposed GaAs streets. Compared to sequential dicing methods, with PDOT, die are separated simultaneously, potentially much faster than the serial process of linear sawing, in which cutting speed is limited to avoid wafer breakage or delamination, especially for wafer thicknesses of 150 µm and thinner. Because of the chemical nature of plasma-based singulation: i) no mechanical force or vibration is applied, reducing the risks of wafer breakage, layer delamination, and lateral damage or chipping, resulting in higher throughput of "good" die with smooth and vertical sidewalls. PDOT is a chemical machining process with no recast or micro cracks

on the sidewalls; ii) the street width can be reduced to 20 µm or less, thereby increasing the number of devices that can be fabricated on a wafer, especially for very small die. This positively affects the ROI and CoO of a plasma dicing tool compared to a mechanical saw; iii) The possibility to separate without failures the die on very thin (≤50 µm) wafers, which cannot easily be separated with other methods.; iv) the use of a vacuum chamber eliminates the operator exposure to highly poisonous dust.

Plasma Dicing on Tape

The PDOT process consists in thinning the wafer at the end of the front-end process and mounting it on a tape frame with the die protected by a photoresist (PR) mask that is applied after thinning. The wafer mounted on tape frame is then inserted in an ICP tool and diced with etching gases such as BCl_3, Cl_2 and $SiCl_4$ (Fig. 1 (a)). The aspect ratio of the streets to etch is definitely an important parameter to consider in plasma dicing because it will impact etch rate similarly to what has been observed in the past for GaAs vias.

In particular, for aspect ratios above 10:1 [6-7], the etch rate can slow down (to approximately 4 µm/min) and consequently, the amount of PR used as a mask becomes an important factor to consider, because it could potentially be fully removed during the plasma dicing process. Well known for GaAs vias, the PR serves two functions: protecting the die underneath during the plasma process and also providing a passivation source for the sidewalls, allowing an anisotropic etch of the features. Plasma polymerization takes place by the high energy plasma reacting with the organic byproducts present in the chamber [8]. In the specific case of PDOT, the polymer source for passivating the sidewalls comes as well from the tape that is exposed to plasma as described in Fig. 1 (b). The combination of the plasma byproducts generated by the PR and the tape is providing the passivation on the sidewalls as illustrated in Fig. 1 (c).

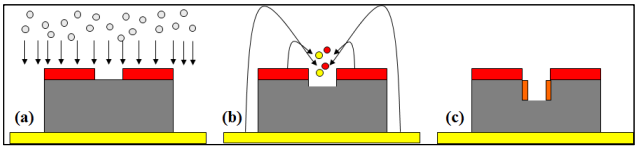

Fig. 1. (a) GaAs wafer mounted on tape with die protected by PR mask and exposed to plasma ions; (b) byproducts generated by the interaction between the plasma gas and the PR mask and the plasma gas and the tape; (c) byproducts deposited on the sidewalls of the streets that are being etched.

Experimental Details

For this work, 3" and different thickness GaAs wafers with 10:1 features and die size of 170µm x 230 µm have been used. The PR choice to mask the die is between 60 µm and 80 µm of SU8. The plasma tool used in this work is a Plasma-Therm Versaline ICP 2 MHz/2500 W with a 13.56 MHz/600 W bias generator.

$SiCl_4$, BCl_3, and Cl_2 have been used in this work as etching gases. Flows, concentrations, power levels and pressure have been varied in order to find the best process conditions to dice GaAs wafers. Process development has been mostly done on full-thickness wafers in order to find the best process conditions for the thinner wafers.

Results and Discussions

Fig. 2 shows an optical image of a GaAs wafer with 40 µm streets at 6:1 aspect ratio in cross section partially diced by using a low flow of BCl_3, medium flow of Cl_2 and a high bias power with an etch rate of ~ 3.6 µm/min. The sidewalls of the die appear to be rough and the PR was completely consumed during the dicing process.

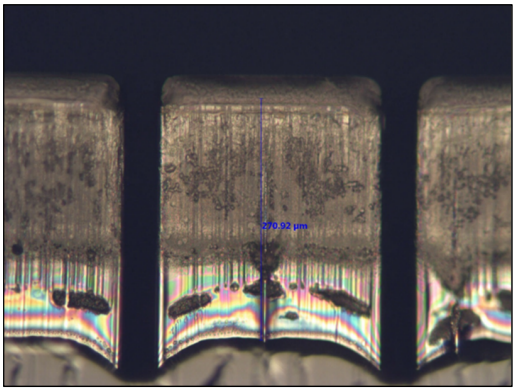

Fig. 2. optical cross section of a full-thickness GaAs wafer with 40 µm streets partially diced to ~ 270 µm depth by using a low flow of BCl_3, medium flow of Cl_2, and a high bias power.

Lowering the bias power and increasing the Cl_2 flow does not seem to reduce sidewall roughness and selectivity as demonstrated in the optical cross section in Fig. 3. The etch rate is comparable to the previous process rate.

Further experiments based on changing the ratio of Cl_2 and BCl_3 and/or the ICP and bias power and/or the pressure did not show any improvement regarding the sidewall quality and the etch rate. Because of that, different etching gases have been explored. In particular, BCl_3 could be replaced by N_2 [8-9] or $SiCl_4$ [10] to enhance the polymerization mechanism created when it reacts with the PR and the tape.

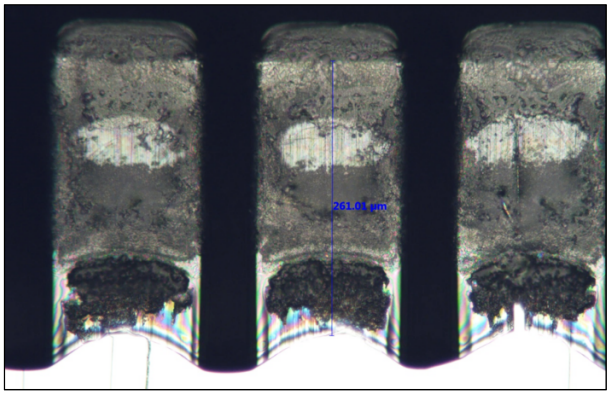

Fig. 3. Optical cross section of a full-thickness GaAs wafer with 40 µm streets partially diced to ~ 260 µm depth by using a low flow of BCl_3, high flow of Cl_2, and high bias power.

Fig. 4 shows an example of GaAs wafer with 40 µm streets at 7:1 aspect ratio in cross section partially diced by using a low flow of $SiCl_4$ and a high flow of Cl_2 with a low bias power. The sidewall quality is definitely improved compared to the previous cases and a large amount of the PR mask is still left (~36 µm). The PR and tape consumption is reduced by adding the $SiCl_4$ because stronger and more efficient polymer chains have been created to protect the sidewalls. This means that a thinner PR mask is required, decreasing the production costs.

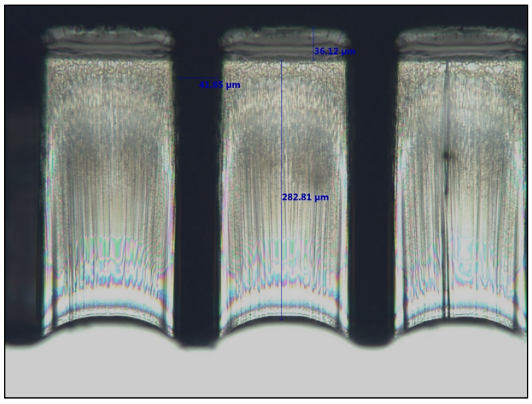

Fig. 4. Optical cross section of a full thickness GaAs wafer with 40 µm streets and aspect ratios near 7:1 (~ 300 µm depth) partially diced by using a low flow of $SiCl_4$, high flow of Cl_2 with a low bias power.

The results achieved by using the $SiCl_4$ on the wafer with 40 µm streets were encouraging in order to adopt this same process on the 20 µm streets wafer. The SEM cross section in Fig. 5 shows that, also on 20 µm streets, the results in terms of verticality of the profile and smoothness of the sidewalls have been achieved with an etch rate comparable to the 40 µm streets wafer.

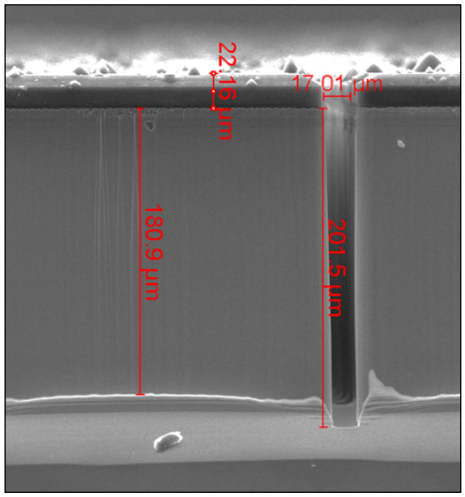

Fig. 5. SEM cross section of full-thickness GaAs wafer with 20 µm streets partially diced to ~ 200 µm depth by using a similar recipe adopted for the wafer in Fig. 4.

The effects of cathode temperature and ICP power have also been studied to quantify their influence on sidewall quality. In particular, the cathode temperature seems to dramatically affect the polymer passivation on the sidewalls, as observed in Fig. 6. It has been observed that at low temperatures, roughness on the sidewall occurs likely due to the poor degree of polymerization, while medium temperatures offer a good compromise for sidewall passivation.

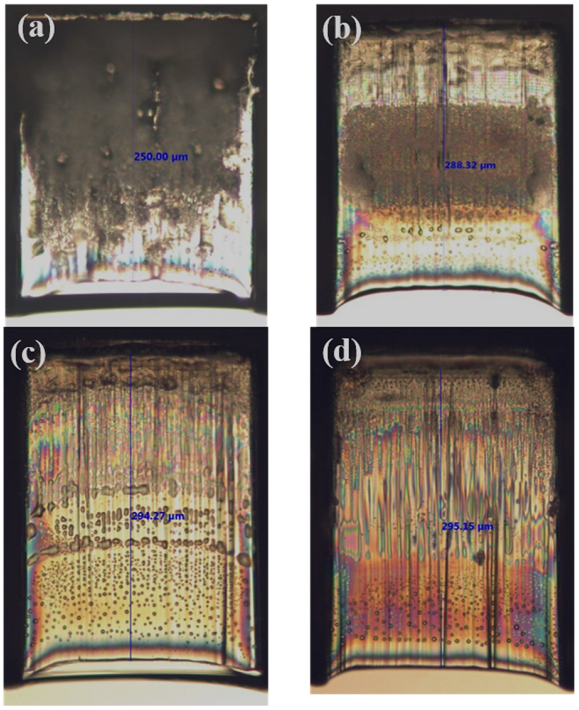

Fig. 6. ESC temperature effect on sidewall quality for full-thickness GaAs wafer with 40 µm streets at ~ 7:1 aspect ratio (~ 300 µm depth). ESC temperature is respectively (a) -10°C; (b) 10°C; (c) 20°C; (d) 30°C.

The ICP power also seems to play an important role in sidewall quality. In fact, high ICP power levels accelerate the polymerization process, allowing a better, thicker, and stronger passivation layer deposited on the sidewalls as shown in Fig. 7.

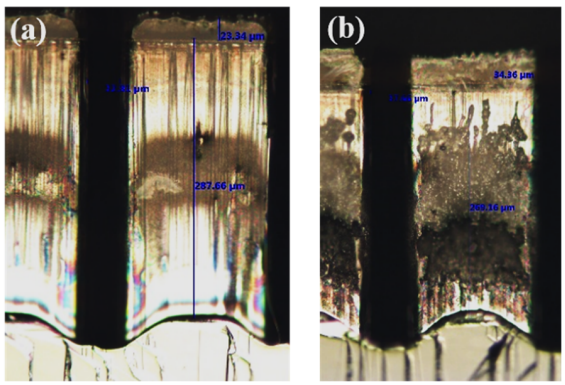

Fig. 7. Influence of ICP power level on the sidewall quality: (a) high power; (b) low power.

INTEGRATION PERSPECTIVE

Although full dicing on tape frame has been developed from an etch standpoint, multiple process integration challenges remain. Further activity optimizing masking schemes and the post-etch cleaning of Cl-containing by-products is ongoing.

Even though the devices presented in this work did not contain back metal, many RFIC devices include a back metal layer that also has to be separated. Since plasma processes are not capable of etching most back metals, an additional separation process will be required. These backmetal separation processes have already been developed for silicon-based devices and are expected to be compatible with many of today's GaAs devices.

Fig. 8 shows an optical micrograph of the back of a plasma-diced wafer where the backside metal has been subsequently removed from the dicing streets.

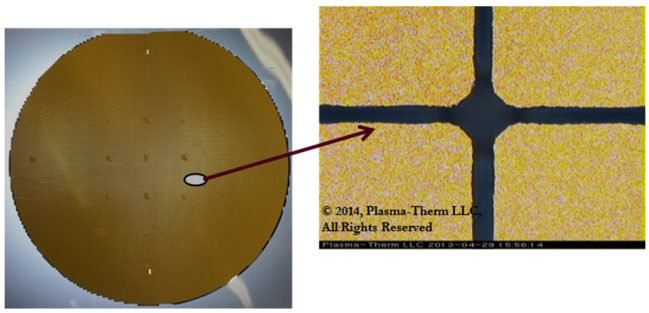

Fig. 8. Plasma-diced wafer with back metal separation after plasma processing (a) wafer on frame – back metal side "up"; (b) optical micrograph of separated back metal.

CONCLUSIONS

This work has shown that PDOT of GaAs can be achieved up to ~ 300 µm depth. The etch rate is ≤4 µm/min especially for a high aspect ratio of 10:1 but, based on the industry trend to make wafers 50 µm thin, PDOT could be a viable solution to replace conventional dicing techniques. In particular, the introduction of $SiCl_4$ in the process seems to help in improving the passivation of the sidewalls and reducing the consumption of the PR mask.

Compared to traditional dicing processes, there are numerous benefits in using PDOT. Especially for thin wafers and small die, the ROI and CoO could be lower compared to traditional dicing techniques that have limitations due to yield loss and street width. However, other limitations have to be overcome to adopt plasma dicing on tape in production for GaAs similarly to what has been done for Si devices. The main limitations are the ability to remove the mask and clean the sidewalls without impacting the device performance and functionality. In addition, back metal separation is still a problem to be addressed.

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ACRONYMS

LED: Light Emitting Diode
MESFET: Metal-Semiconductor Field-Effect Transistor
HEMT: High Electron Mobility Transistor
HBT: Heterojunction Bipolar Transistor
SU8: Epoxy-based photoresist
RFIC: Radio Frequency Integrated Circuit
ESC: Electrostatic Chuck
RoI: Return on Investment
CoO: Cost of Ownership
PR: Photo Resist
TWV: Through Wafer Via
ICP: Inductively Coupled Plasma
PDOT: Plasma Dicing On Tape