# Device Development of Gallium Oxide MOSFETs Grown by MOVPE on Native Substrates for High-Voltage Applications

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**Abstract**

**We summarize the development of β-$Ga_2O_3$ MOSFETs fabricated on homoepitaxy grown by metal organic vapor phase epitaxy including improvements in electrical performance through optimization of doping and thickness, and methods to reduce ohmic contact resistance. We present four development stages of MOSFET data showing progression of β-$Ga_2O_3$ MOSFETs toward high power and potentially high frequency power switching applications.**

## INTRODUCTION

Beta-phase gallium oxide (β-$Ga_2O_3$) is the most promising wide bandgap semiconductor since the maturation of GaN and SiC. The main advantages of β-$Ga_2O_3$ are its wide bandgap (~4.8 eV) and native substrate availability which can be synthesized by melt-growth technology with a wide variation in dopant type and range. These main technical merits position β-$Ga_2O_3$ extremely well for low-defect density homoepitaxial growth of β-$Ga_2O_3$ on cost-effective, large-area substrates for high-voltage applications [1]. β-$Ga_2O_3$ has an estimated critical field strength ($E_C$) of ~8 MV/cm leading to a Baliga's Figure of Merit [2] (~$E_C^3$) for power-switching far surpassing GaN and SiC. Green et al. have already reported a measured $E_C$ = 3.8 MV/cm for a lateral β-$Ga_2O_3$ metal oxide semiconductor field-effect transistor (MOSFET) which surpasses theoretical bulk $E_C$ for GaN and SiC [3]. Further, while the saturation velocity ($v_{sat}$) of β-$Ga_2O_3$ is not well-known, it would need only be ~1/3 of GaN to have a near-equal Johnson Figure of Merit (~$v_{sat} \cdot E_C$) for high-frequency power operation. Initial physics simulation from Ghosh and Singisetti estimate vsat as high as 2.0 x $10^7$ cm/s [4], easily surpassing this requirement. Here, we document our β-$Ga_2O_3$ device development through a series of four fabrication development steps towards monolithically integrated high-voltage devices.

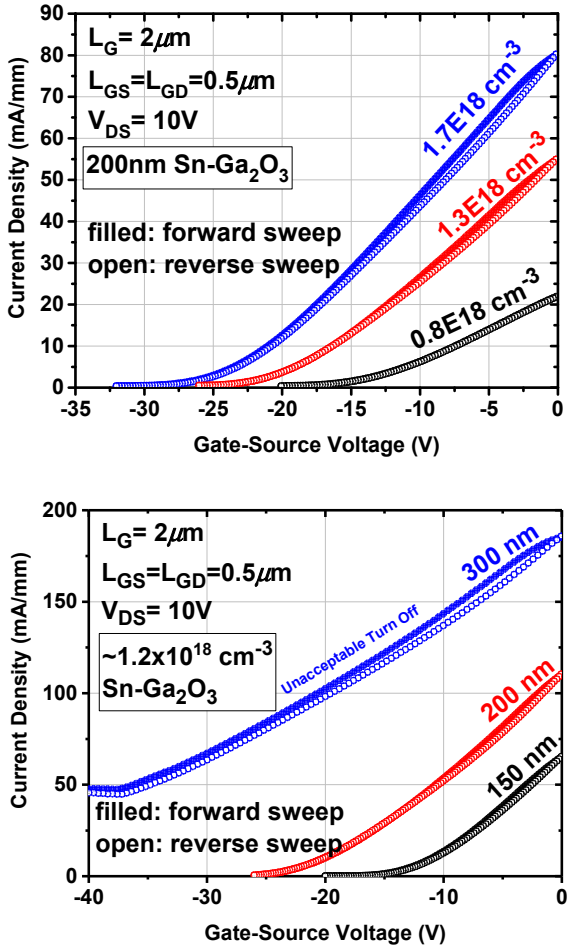


Fig. 1. Transfer curves ($I_{DS}$-$V_{GS}$) of 2nd gen β-$Ga_2O_3$ MOSFETs with varying Sn chemical concentration with constant 200 nm channel thickness (top) and with varying active channel thickness with nearly constant Sn chemical concentration (bottom) showing dependence of threshold voltage and peak current density on both.

## First Generation MOSFETs: Initial Process Development

All MOSFETs were fabricated on n-type channels homoepitaxially grown by metal-organic vapor phase epitaxy (MOVPE) on 10 mm x 10 mm samples. For first generation devices, homoepitaxy was grown on (100) Mg-doped semi-insulating substrates with a Sn chemical concentration of $1.0 \times 10^{18}$ $cm^{-3}$ and a 200 nm layer thickness. First generation MOSFETs used a fabrication process sequence including e-beam evaporated Ti/Al/Ni/Au ohmic contacts without ohmic anneal, plasma-enhanced atomic layer deposited (ALD) 20-nm $Al_2O_3$ gate dielectric patterned by $CF_4$ plasma etching; and an e-beam evaporated Ti/Au gate/interconnect layer with 2-µm gate length ($L_G$).

These devices were used to verify the MOSFET fabrication process, breakdown potential of the β-$Ga_2O_3$ material system, and linearity of ohmic contacts. Transistor operation was confirmed using a manual curve tracer, ohmic contact resistance, $R_C$, was measured with the transfer length method (TLM) to be ~40 Ω–mm with only a few test structures exhibiting good ohmic (linear) behavior, and blocking voltages, $V_{BK}$, of up to 380 V were achieved on devices with a 12 µm gate-drain spacing (G-D). The devices, however, exhibited poor on/off ratios, high-magnitude, negative threshold voltages, $V_{th}$, and inconsistency in the behavior and contact resistance of ohmic contacts.

Additional samples were utilized to improve the on/off ratio from ~$10^3$ to ~$10^7$ by application of a $BCl_3$ inductively coupled plasma (ICP) mesa etch. Improvements to ohmic contact uniformity were also evaluated using a 470□C, 60 sec ohmic anneal in $N_2$ ambient. This improved ohmic linearity and uniformity and also caused a slight improvement with $R_C$ = ~16 Ω–mm for TLM measurements on annealed samples.

## Second Generation MOSFETs: Doping and Thickness Variations

Similar Sn-doped MOVPE grown homoepitaxy on (100) semi-insulating substrates was used for the second series of devices. In this series, channel layers were grown with thicknesses ranging from 150 to 300 nm, and with Sn chemical concentrations ranging from $0.8 \times 10^{18}$ to $1.7 \times 10^{18}$ $cm^{-3}$ to study the effects of these variables on MOSFET performance and optimize threshold characteristics. The second generation MOSFET process included the previously evaluated mesa-isolation by $BCl_3$ ICP etching prior to the ohmic metal deposition and the 1–min ohmic anneal in $N_2$ ambient at 470° C after ohmic metal deposition. These fabrication improvements resulted in both improved on/off ratios with devices achieving $I_{on}/I_{off} > 10^6$ and improved consistency in linearity and resistance of ohmic contacts across each 10 mm x 10 mm sample. $R_C$ ranged from ~10 to ~50 Ω-mm as measured by TLM and varied inversely with the Sn chemical concentration as expected.

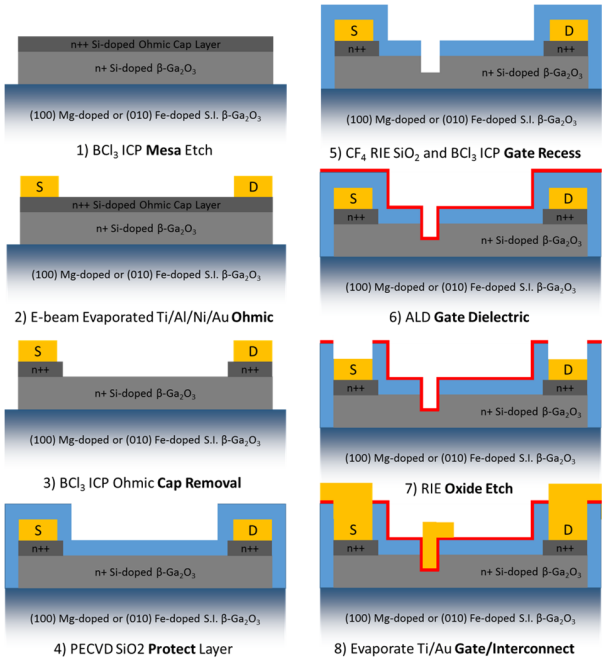


Fig. 2. Gate recess process developed and used for third and fourth generation β-$Ga_2O_3$ devices. The ohmic cap layer is used to reduce the contact resistance and the gate recess narrows the channel to provide desired threshold characteristics. Steps 2, 7, and 8 were used for first generation devices. Steps 1, 2, 7, and 8 were used for second generation devices. An ohmic anneal at 470□ C for 60 sec in $N_2$ ambient followed step 2 for device generations 2-4.

The linear transfer characteristics of second generation devices with doping and active layer thickness variations are shown in Fig. 1. As expected negative threshold voltage ($V_{TH}$) shift and higher current density occurs as the Sn chemical concentration is increased. Likewise, for a given chemical concentration a negative $V_{TH}$ shift and increased current density was measured as the channel thickness increased. For a 300-nm channel with Sn chemical concentration of $1.2 \times 10^{18}$ $cm^{-3}$, large negative voltages applied to the 2-µm gate could not adequately turn off the channel. However, by etching narrow fin channels with a wrap-gate topology, Chabak et al. recently demonstrated a finFET with high-voltage enhancement-mode operation [5] using similar material.

The data in Fig. 1 were further analyzed using Hall effect measurements on van der Pauw structures. These data showed significantly lower active carrier concentration, $N_d$, between $3.4 \times 10^{17}$ and $4.9 \times 10^{17}$ $cm^{-3}$ than the as grown Sn chemical concentration. Sample mobility values varied from 12.4 to 20.9 $cm^2/V \cdot s$ and surprisingly showed a slight variation with $N_d$ rather than the usual inverse variation resulting from impurity scattering effects. On (100) Mg-doped semi-insulating substrates, planar defects have been noted in

literature to severely limit mobility without an optimal miscut angle [6].

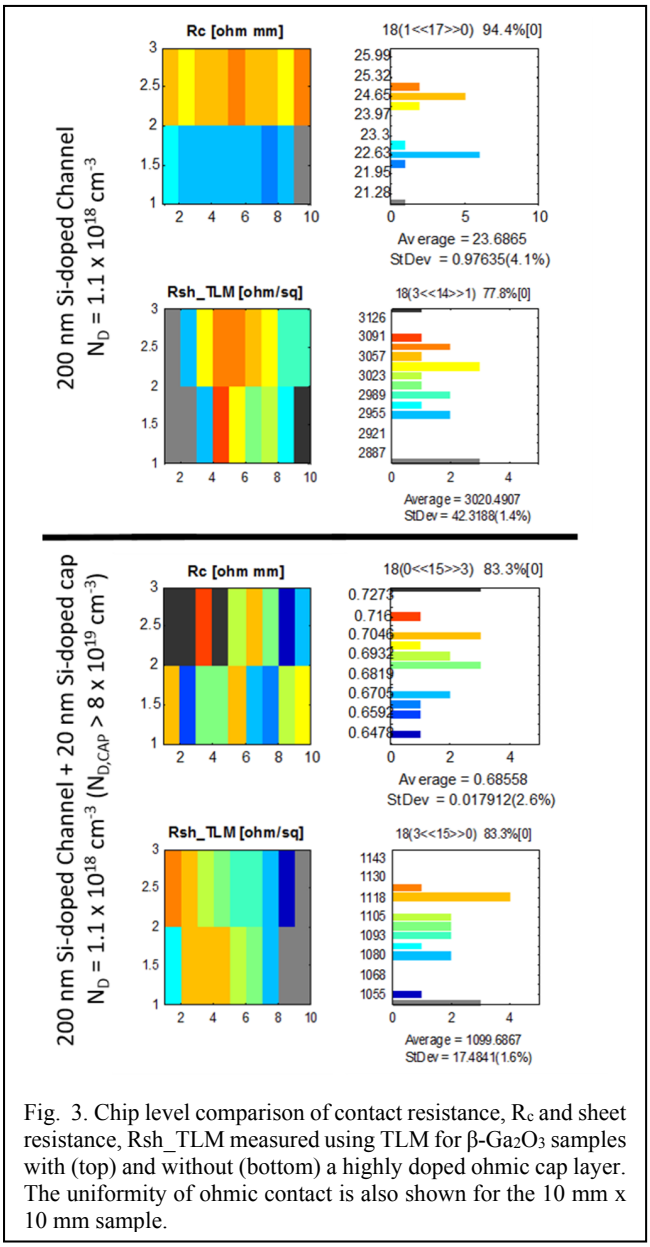


Fig. 3. Chip level comparison of contact resistance, $R_c$ and sheet resistance, Rsh_TLM measured using TLM for β-$Ga_2O_3$ samples with (top) and without (bottom) a highly doped ohmic cap layer. The uniformity of ohmic contact is also shown for the 10 mm x 10 mm sample.

## Third Generation MOSFETs: Gate Recess Process Development and Si Doping

Our third series of devices used Si-doped MOVPE grown channel layers on commercially available (010) Fe-doped semi-insulating substrates [7]. All device channels were 200-nm with Si chemical concentration targeting ~1.0 x $10^{18}$ cm$^{-3}$. Additionally, samples were grown with or without a 20 nm ohmic cap layer degenerately doped with Si to a target concentration of ~8.0 x $10^{19}$ cm$^{-3}$ to reduce ohmic contact resistance. Using these samples we developed a gate recess process that included the previously described mesa and ohmic steps followed by removal of the ohmic cap layer between source and drain ohmics by $BCl_3$ plasma etching, plasma enhanced chemical vapor deposition (PECVD) of 200 nm of $SiO_2$ as a protect mask, a $CF_4$ reactive ion etch (RIE) of the $SiO_2$ to pattern the gate recess dimension, and another $BCl_3$ plasma etch to recess the gate dimension to an adequate depth in the $Ga_2O_3$ to achieve target threshold characteristics based on the previous doping and thickness study. These steps were followed by ALD gate dielectric, patterning, and gate/interconnect evaporation as described previously. The entire gate recess process is shown in Fig. **2**.

While the third series of devices was primarily used for process development, VDP measurements on a sample without an ohmic cap layer after mesa isolation and ohmic contact formation indicated a significantly improved average mobility of 107 cm$^2$/V·s and improved dopant efficiency with $N_D$ ~ 1.1 x $10^{18}$ cm$^{-3}$ being very close to the 1.0 x $10^{18}$ cm$^{-3}$ target chemical concentration. The resulting sheet resistance was $R_{sh}$ = 2.6 kΩ/sq. $R_C$ on this uncapped sample was approximately ~23 Ω·mm using TLM measurements. After employing the same mesa and ohmic process on a capped sample, the $R_C$ and $R_{sh}$ measured using TLM drastically improved to < 0.7 Ω·mm and ~1.1 kΩ/sq, respectively, as shown in Fig. **3**.

Immaturity in the gate recess dimensions required and the improved active carrier concentration limited device performance for this series of samples. A few devices had on/off ratios of >$10^3$ but often exhibited lower than expected on-current indicating over etching of the channel. Most devices with expected current densities did not pinch off at all. The relationship between channel thickness/doping and gate length required for good off-state characteristics needs to be analyzed further. In our case, the increased active carrier concentration with the Si-dopant was unexpected and led to inadequate gate recess for this generation of devices.

## Fourth Generation MOSFETs: Highest Performance and Potential for RF

Our fourth generation devices were fabricated on Si-doped MOVPE grown channel layers on (100) Mg-doped semi-insulating substrates. Substrates had an optimal miscut to reduce planar defects leading to a mobility of ~80 cm$^2$/V·s as measured using Hall effect on sister samples. Epitaxy included a 180 nm channel layer with Si chemical concentration targeted at ~1.0 x $10^{18}$ cm$^{-3}$ and a 25 nm ohmic cap layer with Si concentration targeted at >1.0 x $10^{19}$ cm$^{-3}$. Secondary Ion Mass Spectrometry (SIMS) measurements on similar samples indicated a Si concentration of 1.3 x $10^{18}$ cm$^{-3}$ and 3 x $10^{19}$ cm$^{-3}$ for the channel and ohmic cap layers respectively. The gate recess process shown in Fig. **2** was used to create a ~90 nm channel under the gate, which allowed the use of a shorter gate length of ~0.6 µm at the bottom of the recess etch.

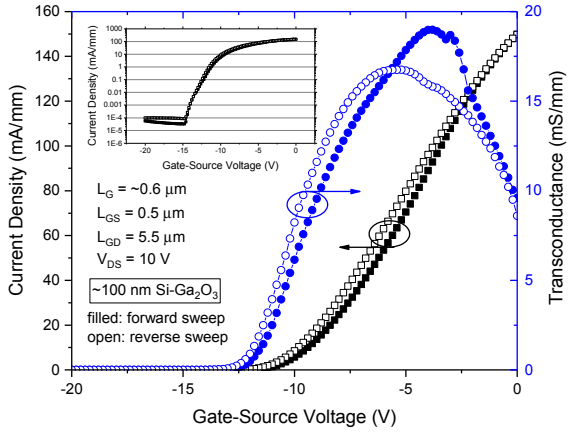


Fig. 4. Transfer ($I_{DS}$ - $V_{GS}$) and transconductance ($G_M$-$V_{GS}$) curves for an Si-doped β-$Ga_2O_3$ MOSFET using a recessed channel. The inset is a log scale plot of the transfer curve showing $I_{ON}/I_{OFF} > 10^6$.

Initial results from these devices indicate significantly improved performance over previous devices including a higher saturation current density at gate voltage of 0 V, IDSS = ~150 mA/mm and higher transconductance, $G_M$=~20 mS/mm while maintaining good $I_{on}/I_{off}$ >$10^6$ characteristics and threshold voltage characteristics, Vth = ~8.5 V. Results of an example device are shown in Fig. 4. The gate recess process enables these changes by allowing channel control with a shorter gate length. TLM measurements showed an $R_C$ = ~2.0 Ω–mm and an $R_{sh}$ = ~3.3 kΩ/sq which is comparable to our best result for third generation devices considering the slightly thinner channel layer (180 vs 200 nm) and the lower chemical concentration in the ohmic cap layer (3 x $10^{19}$ vs. 8x$10^{19}$ $cm^{-3}$). Preliminary RF data on these devices showed transition frequency, fT = ~8 GHz. Additional characterization of these devices is ongoing

## Conclusions

We have shown the results of four device development cycles for β-$Ga_2O_3$ MOSFETs fabricated on n-type channels grown by MOVPE. Ohmic contact resistance was reduced from 40 Ω-mm to ~0.7 Ω-mm by introduction of an ohmic anneal and a highly doped ohmic cap layer. We also introduced a gate recess process which allowed us to maintain good transistor function-as verified by $I_{ON}/I_{OFF}$ > $10^6$-while the active carrier concentration related to the dopant efficiency was improved using Si in the MOVPE growth. Our most recent generation of devices utilized the gate recess process for a ~150 mA/mm device that had both high mobility, ~80 $cm^2/V{\cdot}s$, and high active carrier concentration, ~1.3 x $10^{18}$ $cm^{-3}$, resulting from a better optimized MOVPE growth.

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## Acronyms

AFRL: Air Force Research Laboratory
ALD: Atomic Layer Deposition
ICP: Inductively Coupled Plasma
IDSS: Saturated Drain Current at 0 V gate voltage
MOVPE: Metal organic vapor phase epitaxy
PECVD: Plasma enhanced chemical vapor deposition
RIE: Reactive Ion Etch
SIMS: Secondary Ion Mass Spectrometry
TLM: Transfer Length Method
VDP: Van der Pauw