Advancing Technology with Heterogeneous Integration

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Abstract

The DARPA Microsystems Technology Office (MTO) continues to be at the forefront of the development of revolutionary materials, devices, and integration techniques to meet the performance requirements for advanced microwave and millimeter-wave systems. The Diverse Accessible Heterogeneous Integration (DAHI) program has developed heterogeneous integration processes to intimately combine advanced compound semiconductor (CS) devices and other emerging materials and devices with high-density silicon CMOS technology. This capability has enabled unprecedented circuit performance applicable to DoD systems. The DAHI program has facilitated access to this process through establishment of an integration foundry. In addition to establishing this foundry capability for chip-scale integration, the DAHI program has developed a number of other integration approaches.

Introduction

The compound semiconductor (CS) electronics industry is well-positioned to address the analog challenges of future RF and mm-wave systems, due to the superior properties and diversity of CS materials. For example, the high electron mobility and peak velocity of InP-based material systems have resulted in transistors with fmax above 1THz [1], as well as ultra-high-speed mixed-signal circuits (see, for example, [2]). The wide energy bandgap of GaN has enabled large voltage swings as well as high breakdown voltage RF power devices [3]. The excellent thermal conductivity of SiC also makes power switches at a level of tens of kilowatts possible [4]. Additionally, on-chip high-Q MEMS resonators and switches in materials such as AlN have been demonstrated for potential use for clock references and frequency selective filters [5].

As an example of the potential benefits of heterogeneous integration, consider the plot of Johnson Figure of Merit (product of transistor cutoff frequency and breakdown voltage) [6] versus integrated circuit complexity (as measured by transistor count) for several semiconductor material and device types (Fig. 1). Silicon CMOS is by far the superior technology in terms of integration complexity, exceeding the most advanced CS material (GaAs) by over four orders of magnitude. However, the Johnson FOM for silicon is exceeded by several CS device types by an order of magnitude. Nitride-based semiconductor devices (represented by GaN in Fig. 1) possess the highest Johnson FOM of currently utilized semiconductor materials; however, nitrides have only small-scale integration complexity to date. CS materials such as GaN and InP benefit greatly from leveraging novel silicon-enabled circuit or system architectures to enhance the performance of advanced CS-based RF/mixed-signal circuits.

Given these trends, it is our view that the future of mm-wave electronics depends on heterogeneous integration of compound semiconductors with silicon technology in a way that will allow the advantages of multiple technology types to be optimally combined.

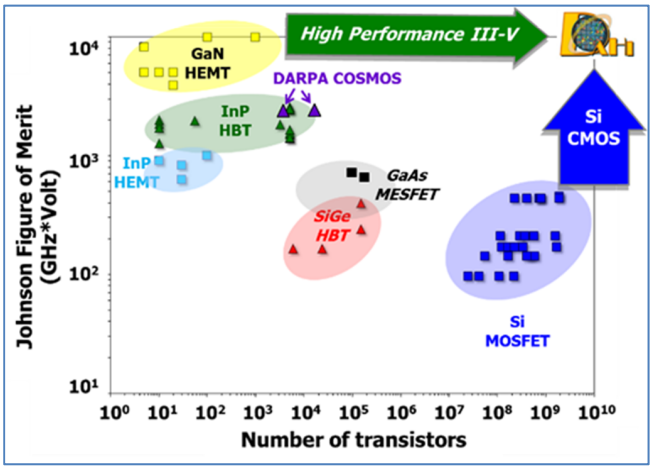

Fig. 1. Plot of Johnson Figure of Merit (product of transistor cutoff frequency and breakdown voltage) vs. Integration Complexity (number of transistors per circuit), classified by a variety of material and device technologies.

Heterogeneous Integration at DARPA

In order to realize the value of heterogeneous integration for DoD systems, DARPA has invested in heterogeneous integration of microwave and mm-wave technology through several programs. The DARPA Compound Semiconductor Materials on Silicon (COSMOS) program, for example, focused on the development of new methods to tightly integrate CS technologies within state-of-the-art silicon

CMOS circuits in order to achieve unprecedented circuit performance levels [7][8][9][10].

The COSMOS program significantly expanded the state-of-the-art in heterogeneous integration technology and demonstrated the potential of this technology for producing revolutionary microsystem capabilities. Building upon this success, the DAHI Foundry Technology thrust was initiated [11] to advance the diversity of heterogeneous device and materials available in a silicon-based platform and make this technology available to the greater DoD and commercial microsystems design community through the establishment of an accessible, manufacturable foundry offering for device-level heterogeneous integration. This foundry includes a wider array of materials and devices (including, for example, multiple semiconductor and MEMS technologies) with complex silicon-enabled architectures on a common silicon substrate platform.

In order to realize this goal of highly flexible, diverse heterogeneous integration, an assembly-based multi-technology integration process was developed. This approach confers a number of important advantages for the establishment of a diverse, accessible foundry technology. By conducting the heterogeneous integration after standard back-end-of-line (BEOL) processing, no process changes are required for the Si base or CS technologies being integrated. This allows rapid introduction of new process technologies within the foundry. Other approaches, in which heterogeneous integration occurs prior to or during BEOL processing, require significant levels of process change, often with extensive process development timescales and budgets. Only a post-BEOL heterogeneous integration approach can allow rapid integration of third-party technologies into a foundry. Additionally, this allows the foundry to easily incorporate advances in Si and CS technology nodes as they become available.

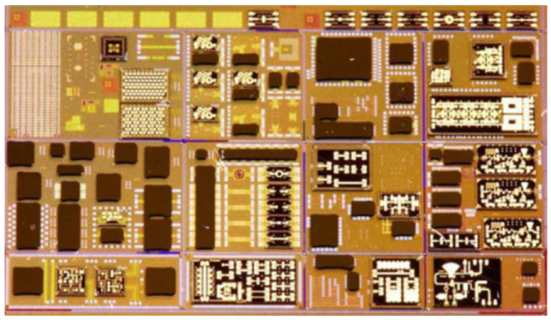

Fig. 2. Micrograph of DAHI multi-project wafer fabricated reticle using a 65 nm base technology (from [12], used with permission).

The first DAHI multi-project wafer run at the DAHI foundry established at Northrop Grumman Aerospace Systems in conjunction with DARPA was completed [12] utilizing 250 nm InP HBTs and 200 nm GaN HEMTs heterogeneously integrated with 65 nm Si CMOS (see Fig. 2). This was the first known instance of heterogeneous integration of three device technologies at the transistor level. This heterogeneous integration process utilized a chiplet assembly-based approach occurring after the completion of BEOL processing. This multi-project wafer incorporated numerous designs, including a heterogeneous integrated Q-Band VCO-amplifier chain [13]. The InP VCO demonstrated 2 GHz of tuning range at 35 GHz while the GaN amplifier provided 15 dB gain.

The DAHI foundry has shown significant progress toward volume manufacturing, including process design kits (PDKs) based on commercial EDA tools, a mature heterogeneous design flow, and good results from yield studies and test vehicles. A second multi-project wafer run consisted of 300 mm Si CMOS 45 nm node wafers serving as the integration platform for InP HBTs and GaN HEMTs (Fig. 3). Seven design teams from the government, academia, and industry contributed novel heterogeneous designs to the program. The collaborative effort with multiple sources of device technologies and designs required sophisticated PDKs and EDA tools for the designers to leverage the varied device features and then integrate the designs for processing.

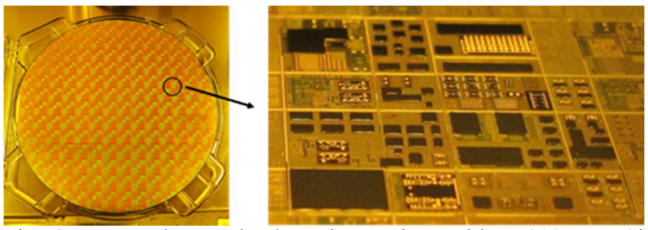

Fig. 3. DAHI three-technology integration, with a 300 mm Si CMOS 45 nm node wafer (left) as the integration platform for InP HBTs and GaN HEMTs (right).

In parallel with the Si CMOS substrate based heterogeneous integration approach, DARPA's DAHI program has explored other integration technologies as well. For example, Teledyne Scientific has demonstrated the integration of 250 nm InP HBTs with 150nm GaN HEMTs using the Direct Bond Interconnect (DBI) wafer bonding process and tungsten vias (Fig. 4) [14]. The device characteristics were shown to be virtually unchanged by the integration process, as illustrated by the before-and-after InP HBT Gummel plots (Fig. 4).

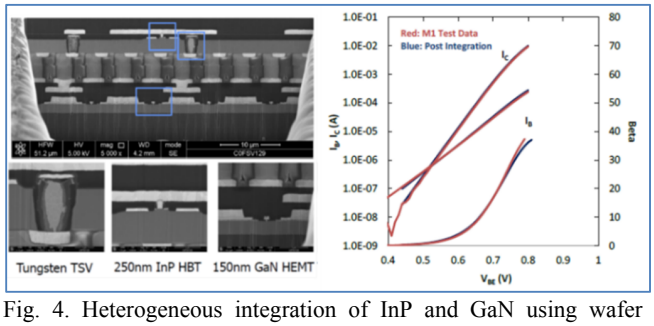

Fig. 4. Heterogeneous integration of InP and GaN using wafer bonding and TSVs (left). The Gummel characteristics of the InP HBT before and after integration (right) show virtually no change due to the integration with GaN devices.

Alternatively, HRL Laboratories has developed a "metal embedded chip assembly" (MECA) technology for integration of multiple device technologies (Fig. 5). The integration platform is a copper base, which makes it an appealing option for high-power applications. Initial results have shown a 2X improvement in power amplifier output power, as shown in Fig. 6 [15].

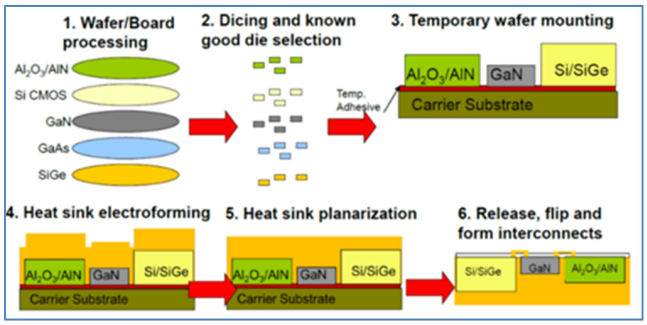

Fig. 5. Metal embedded chip assembly (MECA) enables heterogeneous integration with a metal interconnect platform for high-power requirements. This approach shares features with the wafer-level fan-out packaging technology that is gaining traction in the semiconductor industry [15].

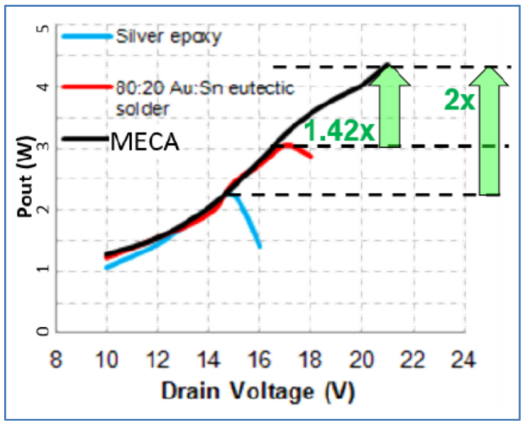

Fig. 6. MECA has enabled up to 2X performance in power amplifier output power due to improved heat transfer [15].

CONCLUSIONS

Heterogeneous integration has the potential to address the challenges present in mm-wave integrated circuit design by combining the superior material properties of compound semiconductors with the integration density of silicon CMOS. DARPA has made substantial investments in developing this capability through the COSMOS and DAHI programs, including the demonstration of revolutionary heterogeneous integrated circuits and the establishment of a foundry capability for heterogeneous integration. It is envisioned that this technology will also enable an unprecedented level of reuse of integrated circuit intellectual property, through the development of standardized integrated circuit chiplets that can be rapidly reconfigured to meet emerging mm-wave integrated circuit needs. It is expected that this will produce a dramatic reduction in design and fabrication cost and development time, thus providing a cost-effective, flexible technology to enable the next generation of advanced mm-wave systems. New initiatives to exploit this promise of design reuse are in progress.

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ACRONYMS

BEOL: Back end of line
CMOS: Complementary metal oxide semiconductor
COSMOS: Compound Semiconductor Materials on Silicon
CS: Compound semiconductor
DAHI: Diverse Accessible Heterogeneous Integration
DARPA: Defense Advanced Research Projects Agency
DBI: Direct bond interconnect
DoD: Department of Defense
EDA: Electronic design automation
FOM: Figure of merit
HBT: Heterojunction bipolar transistor
HEMT: High electron mobility transistor
MECA: Metal embedded chip assembly
MEMS: Micro electromechanical systems
PDK: Process design kit
RF: Radio frequency
TSV: Through silicon via
VCO: Voltage-controlled oscillator