Heterogeneous Integration of Microwave GaN Power Amplifiers with Si Matching Circuits

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Abstract

We integrated GaN high electron mobility transistors into monolithic microwave integrated circuits (MMICs) using hetero-substrates and a redistribution layer (RDL). Driver amplifiers (DAs) and high-power amplifiers (HPAs) on SiC substrates were integrated with matching circuits on Si substrates including through-substrate vias, and connected using a Cu RDL. This was the first attempt to fabricate MMICs with such a structure. This method will be very useful in increasing the achievable quantity of small-size DAs and HPAs—as opposed to using large-size MMICs with matching circuits on a SiC substrate—and in reducing production costs. Furthermore, various frequency bands can be accommodated by changing the Si chips of the matching circuits.

INTRODUCTION

GaN high electron mobility transistors (HEMTs) can be used as high-efficiency high-power amplifiers (HPAs) for wireless communications, radar, etc., because of their tolerance to high-voltage and high-temperature operation [1]. SiC substrates have been widely used in GaN devices—especially in high power applications—because they enable the growth of high-quality epitaxial GaN and have high thermal conductivity, thus contributing to keeping the device temperature down. However, SiC substrates are too expensive for mass production. Some effort is therefore required to reduce production costs.

Few reports have been published addressing the heterogeneous integration of monolithic microwave integrated circuits (MMICs), using Si chips with low-cost and high-performance solutions. Gutierrez-Aitken *et al.* [2] reported on GaN HEMT and InP heterojunction bipolar transistor chips connected onto a complementary metal-oxide-semiconductor (CMOS) wafer using a metal-to-metal thermo-compression process; the thermal resistance of this structure must depend on the thickness of interconnect layers and through-substrate vias (TSVs). Kazior [3] reported that GaN HEMTs were fabricated in windows on Si wafers containing CMOS. In the case of this structure, thermal dissipation must depend on the thickness of the Si substrate, the thermal resistance of Si being several times higher than that of SiC. Margomenos *et al.* [4] reported on the burying of GaN power amplifiers, other integrated circuits, and radio frequency passives into Cu, for thermal dissipation. Kim *et al.* [5] reported that a discrete GaN transistor was embedded in the cavity of a Si interposer, without a mold compound. On the other hand, Sato *et al.* [6] reported having embedded a CMOS power amplifier and chip capacitors into a mold compound, using a redistribution layer (RDL) to connect the components to each other.

In this study, we fabricated an integrated MMIC consisting of a driver amplifier (DA) and an HPA on SiC substrates without TSVs, some matching circuits on Si substrates with TSVs, and a Cu RDL to connect the several substrates, as shown in Fig. 1. This was the first attempt to fabricate an MMIC with such a structure, for low-cost and high-power, because the thermal dissipation of our structure is better than those of GaN-on-Si structures. The contact resistance between RDL and chips, the TSV resistance, the source resistance of the HEMT, the thermal dissipation, and the power characteristics of the resulting hetero-substrate MMIC were investigated.

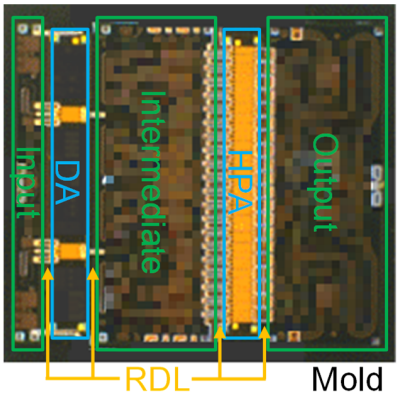

Fig. 1. Surface view of a hetero-substrate MMIC. The RDL consists of Cu wiring to connect each chip. The MMIC size is 6.5 × 7mm^2.

EXPERIMENTAL

Si Matching Circuits

Our MMIC needs to have MIM capacitors with a high voltage tolerance of 150 V. Fig. 2 shows the lifetime predictions on time-dependent dielectric breakdown (TDDB) reliability test of MIM capacitors with a SiN dielectric. The lifetime was estimated by using several models such as the E-model, √E-model, and 1/E-model, as described in ref [7]. It is found that the lifetime will be over 10 years, even if the E-model is used.

In addition, our MMIC need to have high current tolerance. The high current of over 3A flows in the wide interconnects with a width of 80 µm, as seen in the output circuit of Fig. 1. The current density was estimated to be over 1 MA/cm^2, which is too high for interconnects to prevent electromigration (EM). Thus, in order to decrease the current density, the interconnect layers were formed thicker than with the conventional process and the Cu wiring of the RDL was stacked on interconnects of Si chips. The Si chips can then be of benefit in matching circuits of hetero-substrate MMIC.

Process Flow for Hetero-Substrate MMIC

Fig. 3 shows the fabrication process flow for our hetero-substrate MMIC. GaN HEMTs (the DA and HPA) were fabricated on SiC substrates (without backside process TSVs for ground electrodes). The HPA had a maximum drain current (Imax) of 0.6 A/mm and a gate periphery of 38.4 mm. The matching circuits (input, intermediate, and output) consisted of microstrip lines, MIM capacitors, resistors, and inductors, and were fabricated on high-resistive Si substrate with TSVs (formed using a via-middle process) on the surface. The TSV depth was above 100 µm. The chips were mounted on molding tape on the frame with a 50 µm distance between chips, and then molded into a wafer shape. A Cu RDL with spin-on dielectric (SOD; k = 5.1) was formed on the molded pseudo-wafer, to electrically connect the chips. The HEMTs' source electrodes were connected to the TSVs on the Si substrates. The backside of the pseudo-wafer was grinded to a thickness of 100 µm, leaving the TSVs exposed on the backside surface. Ti and Au were deposited on the backside surface, and AuSn solder was used for die bonding to the package.

RESULTS AND DISCUSSION

Contact Resistance between RDL and Chips

Fig. 4 shows the contact resistances between Cu/Ti of the RDL and the bonding pad of Si matching circuits. Generally, the surface material of the IC's bonding pad is Al. As shown in Fig. 4 (a), the contact resistance between Cu/Ti and the Al surface was very high (>1Ω), because the Al surface was oxidized during the RDL processes, such as ref [8]. In order to prevent oxidation of the Al surface, TiN on Al was remained when the pads were opened by etching a passivation layer, although TiN was usually removed.

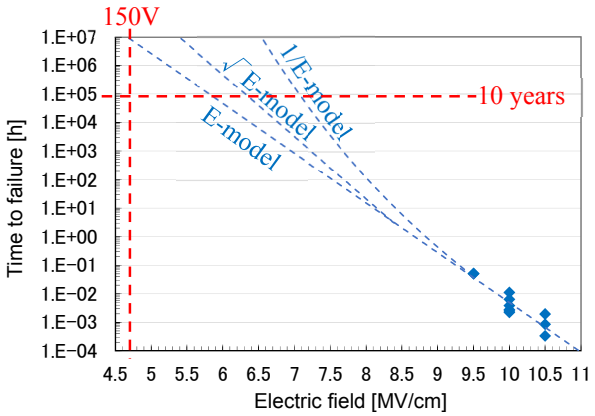

Fig. 2. Lifetime predictions on TDDB of MIM capacitors.

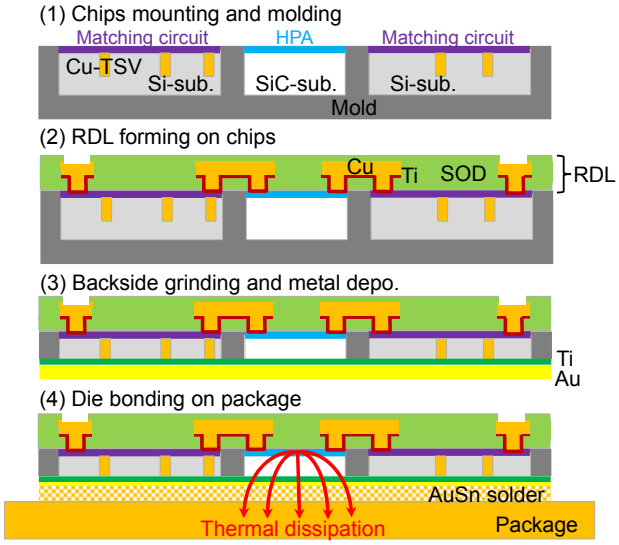

Fig. 3. Process flow for fabricating a hetero-substrate MMIC with Cu RDL.

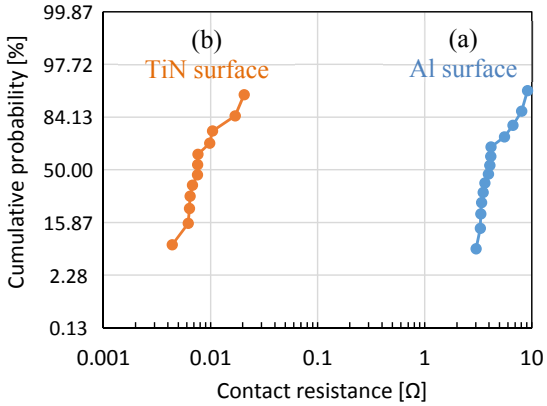

Fig. 4. Cumulative probability distributions of contact resistances between Cu/Ti of RDL and bonding pad of Si matching circuits.

Moreover, TiN is known to be a good diffusion barrier of Cu [9]. As shown in Fig. 4 (b), the contact resistance between Cu/Ti and TiN/Al becomes less than 10 mΩ (median).

TSV Resistance

Fig. 5 shows the resistances of TSV before and after improvement. As shown in Fig. 5 (a), the TSV resistance was high before improvement. One of the causes was the occurrence of large voids caused by air entrainment. Another was micro voids caused by diffusion of AuSn solder to TSV-Cu.

Fig. 6 shows the X-ray transmission image after die bonding using AuSn solder. Black squares and points indicate the position of chips and TSVs, respectively. A lot of voids in the AuSn solder were observed as bright contrast regions. The resistance of TSV on the void was higher than that on AuSn solder.

Fig. 7 shows the cross-sectional EDX mapping for the bottom of the TSV depending on the thickness of the Ti barrier layer. When the barrier layer of Ti was 70 nm thick, it is clearly seen that AuSn solder diffused into the TSV-Cu. On the other hand, it is noted that thick Ti of 200 nm was able to prevent the diffusion of AuSn solder into the TSV-Cu. As shown in Fig. 5 (b), TSV resistance decreased less than 2 mΩ after these improvements.

Source Resistance of HEMT

Fig. 8 shows the cross-sectional schematic of source resistances of HEMT. The resistance is composed of (1) a contact resistance between the RDL and SiC chip, (2) a resistance of Cu wiring of the RDL, (3) a contact resistance between the RDL and Si chip, and (4) a TSV resistance. These resistances were estimated to be (1) 2 mΩ, (2) 12 mΩ, (3) 3 mΩ, and, (4) 2 mΩ, considering the contact areas and length/width of wiring. Thus, the total resistance of these factors is calculated to be about 20 mΩ. It is found that this value has no effect on the power characteristics of MMIC by using a simulation.

Thermal Dissipation of Hetero-Substrate MMIC

Fig. 9 shows the thermal resistance of an HPA on a 5.5 × 0.8 mm^2 SiC substrate of a hetero-substrate MMIC, and that of an identical HPA on a 5.5 × 5 mm^2 wide SiC substrate. The thermal resistances of both HPAs were almost equivalent, even though the SiC widths were considerably different. One may therefore conclude that the thermal dissipation capability is mostly determined by the structures and materials under the GaN HEMT, and is almost independent of the SiC substrate width.

Power Characteristics of Hetero-Substrate MMIC

Fig. 10 shows the output power and the power added efficiency (PAE) of hetero-substrate MMICs. Before improvement, their values were very low, because of high contact resistance and high TSV resistance. After improvement, the hetero-substrate MMIC achieved a PAE of

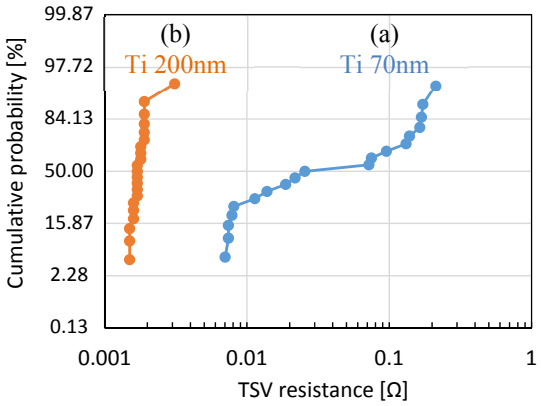

Fig. 5. Cumulative probability distributions of TSV resistances after die bonding using AuSn solder.

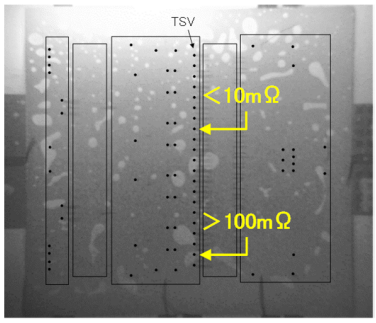

Fig. 6. X-ray transmission image after bonding a die using AuSn solder.

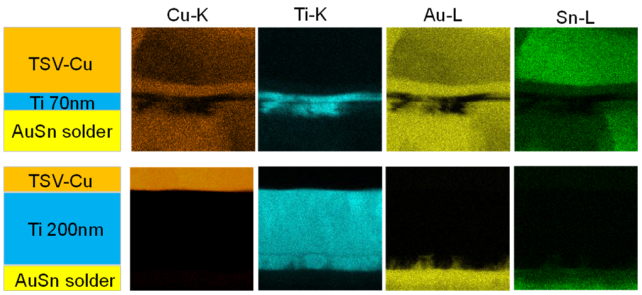

Fig. 7. Cross-sectional EDX mapping for the bottom of the TSV depending on the thickness of the Ti barrier layer.

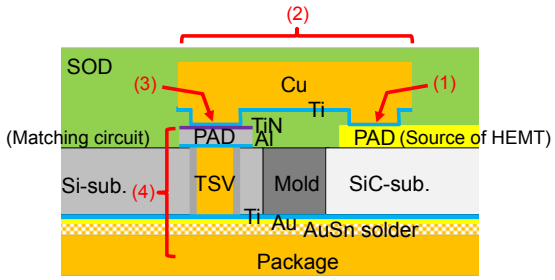

Fig. 8. Cross-sectional schematic of source resistances of HEMT.

37 %, and an output power of 120 W at 3.2GHz, which was less than what was expected. However, when we try to adjust the lengths of microstrip lines by using wire bonding without molding and RDL, their values improve close to what was expected. Therefore, these values will be improved by adjusting the distance between chips and the wiring length of the matching circuits on the Si chips.

CONCLUSIONS

We have performed a heterogeneous integration of GaN HEMTs on MMICs, using RDL technology. The contact resistance between RDL and chips became less than 10 mΩ by remaining TiN on bond pads. TSV resistance decreased less than 2 mΩ with the thicker Ti barrier layer to prevent the diffusion of AuSn solder into the TSV-Cu. The source resistance of HEMT with TSV in Si chips has no effect on the properties, like a HEMT with TSV in SiC chips. The thermal dissipation of the hetero-substrate MMIC was as good as that of an MMIC on a SiC substrate. The values of output power and PAE exhibited by the fabricated hetero-substrate MMIC will be improved by adjusting the parameters of the matching circuits. The proposed technology will certainly be very useful in GaN HEMT MMICs production.

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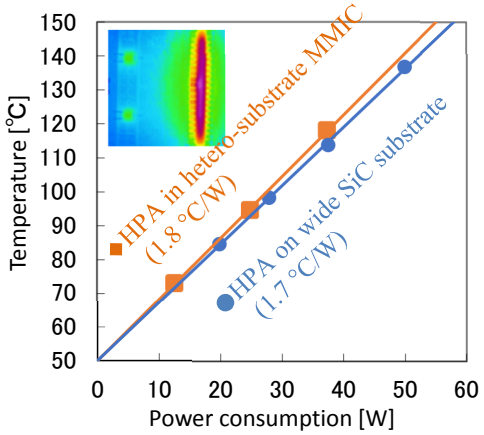

Fig. 9. HPA thermal resistance for different substrate types. Infrared temperature measurements, at a stage temperature of 50 °C.

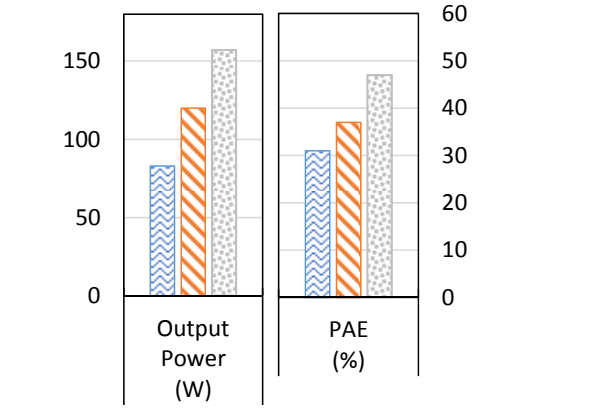

Fig. 10. Output power and PAE of hetero-substrate MMIC.

ACRONYMS

CMOS: Complementary Metal-Oxide-Semiconductor
DA: Driver Amplifier
EDX: Energy dispersive X-ray spectrometry
EM: Electromigration
HEMT: High Electron Mobility Transistor
HPA: High-Power Amplifier
MIM: Metal-Insulator-Metal
MMIC: Monolithic Microwave Integrated Circuit
PAE: Power Added Efficiency
RDL: Redistribution Layer (Cu wiring to connect chips)
SOD: Spin-On Dielectric
TDDB: Time-dependent dielectric breakdown
TSV: Through-Substrate Via