Chemical Attack of a pHEMT Channel Due to Poor Passivation Coverage

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Abstract

This paper outlines the root cause analysis of a fabrication process-induced channel attack of a 130nm pHEMT product. The wafer scrap and die sort yield loss was catastrophic for a product in a pre-ramp stage. Entire wafer scraps occurred due to numerous out-of-spec DFET-related parameters measured on process control monitor (PCM) test structures at both DC and RF test points. Additionally, wafers passing the PCM test, suffered significant yield loss at product die sort testing related to low current. Initial investigation revealed these failures to be more than parametric in nature, possibly defect related. Samples were brought to failure analysis to determine the cause of the failing FETs.

A focused ion beam (FIB) cross-section revealed the epi layers under the gate and ohmic contacts had been attacked and eroded. The eroded channel easily explained the parametric failures. Further analysis revealed seams in the conformal silicon nitride layer that covers the gate; a potential passageway for wet chemistry to penetrate and cause damage to the FET.

INTRODUCTION

In semiconductor manufacturing, yield analysis and root-cause investigations are necessary to improve yields and reliability. Yield improvement can have a positive impact on time-to-market, increased profit margins, on-time delivery to the customer, and guaranteed performance and reliability. At a new product launch, it is critical to investigate failures, determine the root-cause and implement a fix, all before ramping the product.

This paper will outline the process used to find the origin of a defect causing catastrophic yield loss and wafer scrap. Using parametric analysis, wafermap review, process flow dissection, and experimentation. It will continue by discussing the discovery of the root-cause was discovered and how a permanent fix eliminated any chance of reoccurrence.

PARAMETRIC FAILURES

This first sign of a problem came from Product Engineering, where one of the first pre-production lots exhibited significant yield loss at RF die sort test. The failing parameter was a test of the output current from one of the amplifiers in the circuit, where regardless of the gate voltage applied, there was no output current. This implied something severe had happened to the device during manufacturing, likely to be defect related, not parametric.

Wafermaps from die sort test were generated and analyzed for patterns. Wafermaps are a way to view a parametric test data as a function of X, Y location on the wafer, see Figure 1. The yield loss had a peculiar pattern, thus assistance from Fab Yield and Integration Engineering was required. The team went to work determining where the failures originated in the manufacturing process. The yield loss pattern revealed failures concentrated in the center of the wafer, and often so severe, the entire wafer was impacted, see Figure1.

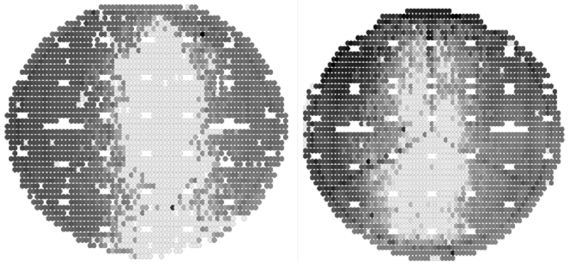

Fig. 1. Examples of wafer maps from two low yielding wafers at product RF Die Sort. The light grey regions down the center of both wafers show failures due to low drain current.

Analysis of the PCM data also showed the problem even before die sort, and gave a clearer signature that the failures were not of normal parametric behavior, but behaved rather catastrophic in nature as they were so far out of the normal distribution, perhaps pointing to a processing defect.

DC parameters are tested at nine PCM's on each wafer, first just after the FET ohmic contacts are formed and again at the end of the line. Failing sites revealed FETs exhibiting low drain current, high on-channel resistance, and positive Vp (Figure 2, left). Thirty-three sites are tested at RF PCM test step. This added resolution showed the similar failure pattern found at die sort. These failures were mainly low FT (Figure 2, right).

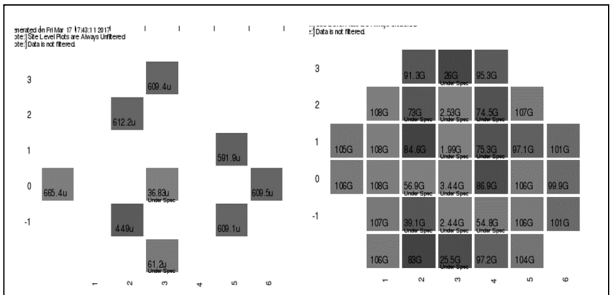

Fig. 2. On the left, DC PCM test failures in center and bottom test keys. On the right, RF PCM, where more sites are tested, shows better resolution that the problem exists down the center of the wafer (lighter grey areas). The center sites are failures and the outer portions of the wafer are not impacted.

Curiously, analysis of DC PCM data taken at the first ohmic test point, did not show any sign of the problem. This clue would later aid in the pursuit of the root-cause of the defect.

Failure Analysis

Knowing that the PCM test structures exhibited a similar parametric signature as the failing die in the circuit, made failure analysis significantly easier, as there was not any need to isolate the failure in the circuit.

A wafer with low yield was submitted for failure analysis. The failing FET was probed to validate the failure and the curve trace analysis showed the inability to produce sufficient drain current. Emission microscopy of the FET was performed to find the exact location of the defect. A focused ion beam (FIB) was used to cut through the defective area of the FET; specifically, a section of the gate. After the FIB cut, the sample was prepared and a Scanning Transmission Electron Microscopy (STEM) provided a high-resolution image, see Figure 3.

The STEM image in Figure 3, revealed a void under the gate, however the gate was not recessed into the void. Since the gate is deposited via a sputter process, the gate should conformally cover any topography. Therefore, the void in the Schottky contact, seemed to form after the gate metal was deposited. Additional SEM cross sections were required to outline the scope of the erosion.

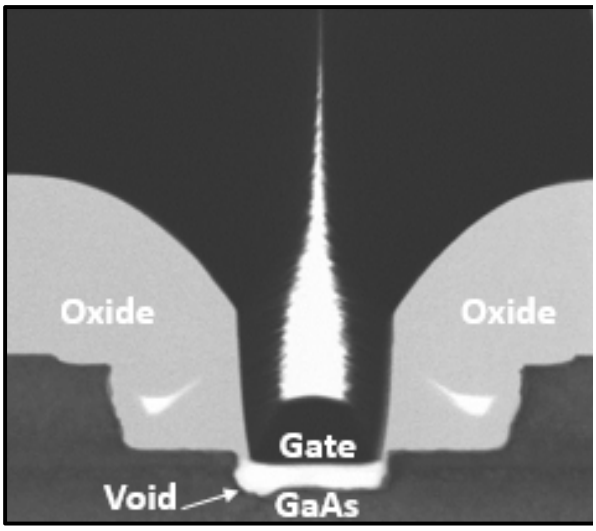

Fig. 3. STEM image of the DFET gate. The area under the gate is a void (bright white) in the GaAs. Note the gate metal does not fill the void.

Additional FIB cuts were performed in systematic intervals along the gate width. This analysis showed more extensive GaAs erosion; not only under the gate but under the source and drain ohmic contacts. There was additional attack of the ohmic metal noted as well, see Figure 4.

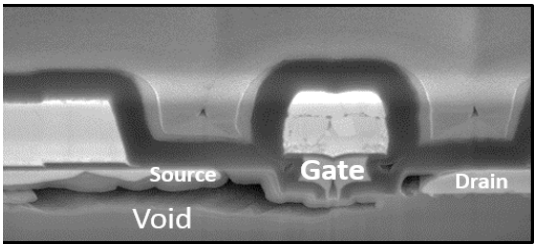

Fig. 4. FIB-SEM image of the DFET gate further along the gate length from the original STEM site in Figure 3. The area under the gate is a void in the GaAs. There is extensive GaAs erosion and attack of ohmic source and drain metal.

Investigation of Defect Origin

Armed with the results of the FIB-SEM and STEM images, showing GaAs erosion under the gate and ohmic, apparently post gate formation, a detailed review of the process was started. Reviewing historical PCM data, the failures did not occur at the inline ohmic (or first) test point. Therefore, the attack

occurs somewhere between ohmic and end fab processing, where a second PCM test is employed and failures were observed.

Since a chemical attack of the Schottky was suspected, all the fabrication steps which involved water or chemical exposure to the wafer were compiled into a list. The difficult part to understand was that right after the inline ohmic test point, there is a silicon nitride (PSN) deposition that completely encapsulates the transistor gate, source and drain. If processing chemistry was attacking the devices, this implied the film coverage was marginal or had cracks. One model suggested water exposure was a potential cause, so engineering wafers were subjected to a water rinse and IPA dry over four consecutive cycles; trying to exaggerate the problem. The wafers did not show any signs of degradation.

Performing a simple IS / IS-NOT exercise, revealed that a very similar high-volume 130nm gate p-HEMT "sister" process flow, was free from any degraded FETs. This indicated there is something subtle yet significantly different in the process sequence between the two fab flows. Examination of the process steps of the two flows side-by-side, showed similar steps regarding metal deposition, metal liftoff, cleans, and etches. The primary difference between the two, is an extra solvent strip process and a 1800A PSN deposition on the "sister" process, see Table 1 for a side-by-side list of process sequences.

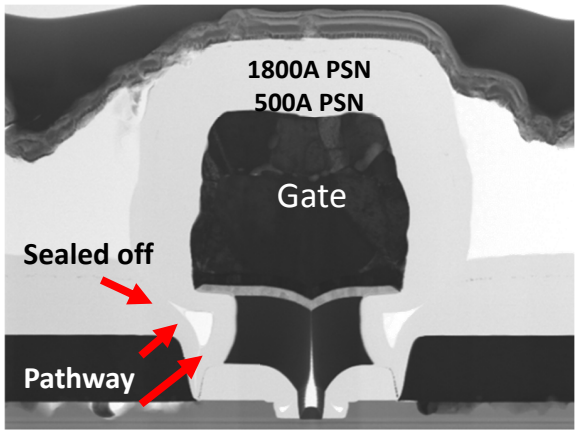

Fig. 5. STEM cross-section of a gate from the process with failures outlined in Table 1. Passivation is seen as light gray layers surrounding dark gate metal. A proposed path down to the GaAs is shown.

TABLE 1
SIDE-BY-SIDE COMPARISON OF SPECIFIC PROCESS STEPS POST OHMIC FORMATION BETWEEN SIMILAR PROCESSES WITH AND WITHOUT FAILURES.

PROCESS WITHOUT FAILURES	PROCESS WITH FAILURES
500A PSN	**500A PSN DEP**
PHOTO	Module does not exist
METAL DEP	
LIFTOFF	
SOLVENT/QDR	
1800A PSN	
PHOTO	PHOTO
DRY ETCH	DRY ETCH
SOLVENT/QDR	**SOLVENT/QDR**
PHOTO	PHOTO
METAL DEP	METAL DEP
SOLVENT/QDR	**SOLVENT/QDR**
PHOTO	PHOTO
METAL DEP	METAL DEP
SOLVENT/QDR	**SOLVENT/QDR**
1200 PSN DEP	**1800A PSN**

DEFECT ELIMINATION

After the side by side comparison was completed, it became clear that the 500A of PSN deposited post ohmic formation, was not robust to the subsequent processing steps. Most likely, the topography of the FET causes seams in the PSN which allowed the passage of processing chemistry. The failure model can be visualized with the aid of a STEM cross-section seen in Figure 5, where a Transmission mode image shows the passivation surrounding the gate of the transistor. The passivation here is a stack of 500A + 1800A deposited after numerous steps shown in Table 1. The water and solvent steps can leave some chemistry in the PSN seams formed at the 500A dep. The seams are due to high topography (V shaped troughs) and a thin PSN layer. Water and the solvents trapped combine to form carboxylic acid, which may further attack the passivation cracks. Combine this with numerous water and solvent modules, a continual attack of the PSN and the underlying GaAs occurs. It was already shown that water alone does not cause the degradation, so it seems that both water and solvent cycles are critical.

The ultimate fix to the attack of the FETs was to mimic the "sister" process through these steps, but to also add some margin. The process change was to deposit the final stack of 500A + 1800A but all together post ohmic contact formation. Keeping with an existing stack thickness target allowed the use of existing etch recipes from the "sister" process.

Split lots, wafers with old process and the proposed changes, were manufactured and the final test data was compared. The proposed changes allowed the FET to be processed without degradation and all yields recovered throughout the test chain. The improved process allows for not only higher yields, but improved quality and reliability, and increased fab (not starting extra wafers) and test capacity (not wasting test time on bad die).

CONCLUSION

This paper has demonstrated the importance of reacting quickly to a pre-production ramp major yield loss. Data analysis which correlated RF die sort fallout back to easily identifiable DC structures and rapid failure analysis, allowed for the generation of a failure model. Employing an IS/ NOT-IS analysis, enabled the identification of a weakness in process margin of a PSN layer in a pHEMT process. The marginality allowed for a combined water and solvent attack of the underlying GaAs and contacts contributing to the yield issue. Quick-turn experiments permitted an elegant solution that was rapidly woven into production which allowed a high-yielding ramp. This is a perfect example of improved process margin leveraging improved metrics at all operations steps across multiple factories.

ACKNOWLEDGEMENTS

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ACRONYMS

pHEMT: pseudomorphic high-electron mobility transistor
DFET: Depletion-mode field effect transistor
PCM: Process Control Monitor
PSN: Silicon Nitride
GaAs: Gallium Arsenide
SVIA: Substrate Via