Engineering PECVD SiN Passivation Layers to Enable AlGaN/GaN HEMTs with Low Leakage, Low Current Collapse and High Breakdown Voltage

A. D. Koehler, T. J. Anderson, M. J. Tadjer, K. D. Hobart, and F. J. Kub

U.S. Naval Research Laboratory, 4555 Overlook Ave. S.W., Washington, D.C., 20375
e-mail: andrew.koehler@nrl.navy.mil, Phone: +1 202-404-6788

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Abstract

The properties of composite plasma enhanced chemical vapor deposition (PECVD) SiN passivation layers, deposited on the surface of AlGaN/GaN high electron mobility transistors (HEMTs) are engineered to achieve low leakage current, low current collapse, and high breakdown voltage devices. High frequency (13.56 MHz) plasma, mixed frequency with alternating high and low frequency (100-360 kHz) plasma were varied to reduce off-state leakage current, improve dynamic on-resistance, and extend the breakdown voltage. Annealing high frequency SiN at 750 °C for 30 minutes improves the breakdown voltage and reduces off-state leakage. This ex-situ deposited and annealed high frequency SiN can also serve as a gate insulator to reduce gate leakage current. Reducing the thickness of the annealed HF SiN degrades the dynamic response, but improves the off-state breakdown voltage.

INTRODUCTION

Effective surface passivation of AlGaN/GaN high electron mobility transistors (HEMTs) is essential for achieving devices with high performance and reliability. Plasma enhanced chemical vapor deposition (PECVD) SiN is commonly used to passivate surface states in AlGaN/GaN HEMTs. Previously, a bi-layer PECVD SiN passivation scheme had been developed to improve the dynamic on-resistance when compared to a conventional mixed frequency PECVD SiN [1]. This bi-layer stack consists of a 10 nm high frequency (HF) at SiN layer, which is deposited before 100 nm of mixed frequency (HF/LF) SiN. The intermediate HF SiN layer suppresses ion bombardment damage of the AlGaN surface during the low frequency (LF) deposition of the low-stress mixed frequency SiN, similar how *in situ* grown SiN does [2]. However, GaN HEMTs passivated with bi-layer PECVD SiN lack desirable breakdown voltage. Effective passivation is critical, as damage occurring during exposure to irradiation creates additional charge traps degrading the dynamic performance more [3]. In this work, a systematic engineering of ex-situ deposited PECVD SiN films is performed to optimize the leakage current, current collapse, as well as breakdown voltage.

EXPERIMENT

All of the AlGaN/GaN HEMT samples that are under investigation were fabricated from a single HEMT epitaxial wafer with GaN / $Al_{0.27}Ga_{0.73}N$ / GaN (2 nm / 17.5 nm / 1.8 μm) wafer on a (111) Si substrate. Device isolation was performed by Cl_2-based inductively coupled plasma (ICP) etching mesas. Ohmic contacts were formed by evaporating 20/120/40/50 nm of Ti/Al/Ni/Au and rapid-annealed at 850 °C for 30 sec in N_2. Schottky gate metal were formed by evaporating 20/200 nm of Ni/Au. Probing contact pads were formed by 20/200 nm of Ni/Au. Passivation with SiN was performed either before or after the Schottky gate formation. An SF_6 ICP etch was used to open contact windows in the SiN passivation layers. Before passivation, a cleaning procedure consisting of 10 min UV-O_3, followed by 30 sec 1:10 HCl:H_2O, and 30 sec 10% buffered oxide etch (BOE). The device dimensions were gate length of 3 μm, gate-source spacing of 2.5 μm, and a gate-drain spacing of 10 μm.

The mixed frequency (HF/LF) SiN recipe was optimized for low stress and uniformity in thickness and refractive index across the wafer. An Oxford Instruments PlasmaLab100 PECVD system was used with a recipe of 300 °C, 20 W, 650 mT, 20 sccm SiH_4, 23.5 sccm NH_3, 980 sccm N_2, with alternating HF for 13 sec and LF for 7 sec. This resulted in a deposition rate of ~12 nm/min with near stoichiometric SiN refractive index (1.98-2.01).

As summarized in Figure 1, ten splits in PECVD SiN surface passivation were performed. This includes a) an unpassivated reference, b) HF/LF SiN passivation, c) a bilayer SiN with a 10 nm HF interlayer and 100 nm of HF/LF, d) HF SiN before gate, as a gate dielectric, e) HF SiN annealed at 750 °C before gate, f) HF SiN before gate with additional bilayer SiN after gate, g) HF SiN annealed at 750 °C before gate with additional bilayer SiN after gate, h) HF SiN annealed at 750 °C before gate with additional mixed frequency SiN after gate, i) 5 nm thick HF SiN annealed at 750 °C before gate with additional mixed frequency SiN after gate, and j) 5 nm annealed at 750 °C HF SiN annealed at 750 °C before gate with additional mixed frequency SiN after gate.

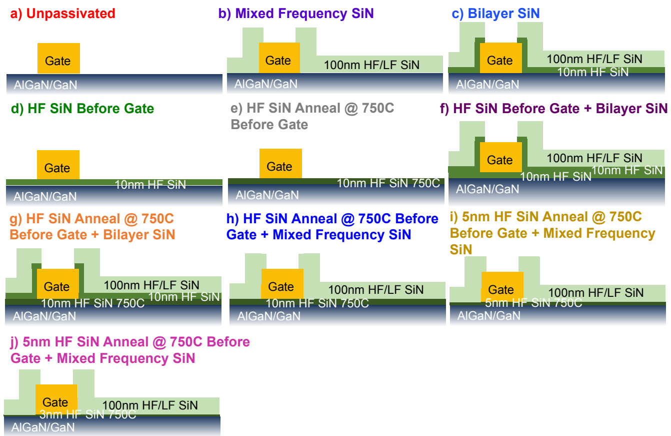

Fig. 1. Schematic cross-sections of various passivation schemes on the surface of AlGaN/GaN HEMTs, which are investigated.

Results & Discussion

As shown in Figure 2, the dynamic on-conductance (Dynamc G_{ON}) is extracted from pulsed I-V measurements with 500 ns pulses to the on-state with 1 ms at various drain quiescent voltage. Unpassivated HEMTs (Sample a) have poor dynamic response, due to severe charge trapping in the access region between the gate and drain. Mixed frequency SiN (Sample b) has improved dynamic G_{ON}, and the bilayer (Sample c), has even better current collapse.

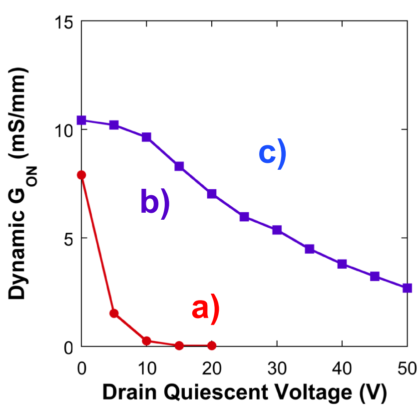

Fig. 2. Unpassivated HEMTs shows poor dynamic on-conductance compared to mixed frequency SiN passivated HEMTs and the benefit of bilayer SiN in improved dynamic on-conductance is evident compared to conventional mixed frequency PECVD SiN.

Although Sample c has good dynamic response, Figure 3 shows the breakdown for Sample c is low (~360 V). The impact of the HF SiN is investigated independently, by implementing 10 nm of HF SiN before gate (Sample d) and annealing the 10 nm of HF SiN at 750 °C before gate (Sample e). This anneal densifies the SiN. As shown in Figure 3, unannealed HF SiN is poor for breakdown, as Sample d has extremely low breakdown (~80 V). However, the annealed HF SiN extends the breakdown voltage to 580V.

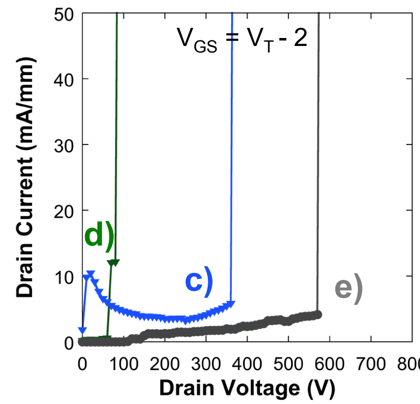

Fig. 3. Unannealed HF SiN yields poor breakdown voltage but annealed HF SiN is beneficial for breakdown.

Figure 4 shows the dynamic on-conductance tradeoff between Samples c, d, and e. Although Sample e has good breakdown (Figure 3), the dynamic response (Figure 4) is poor. The opposite is true for Sample d, which has poor breakdown but excellent dynamic behavior. Sample F has breakdown voltage around 5 V, and is essentially unusable, this indicates that thicker unannealed HF SiN is electrically leaky and detrimental to the breakdown strength. However, Sample g shows good breakdown characteristics, comparable to Sample e, and good dynamic response as shown in Figure 5.

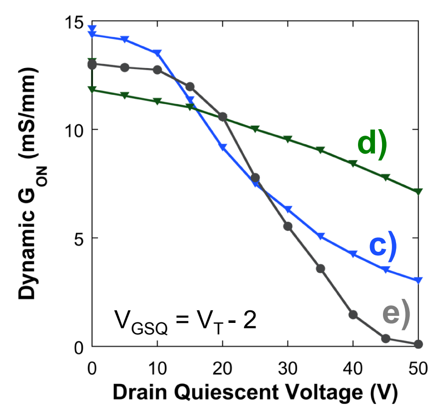

Fig. 4. Annealed HF SiN alone is insufficient at passivating the access regions, but unannealed HF SiN, as shown by the dynamic on-conductance.

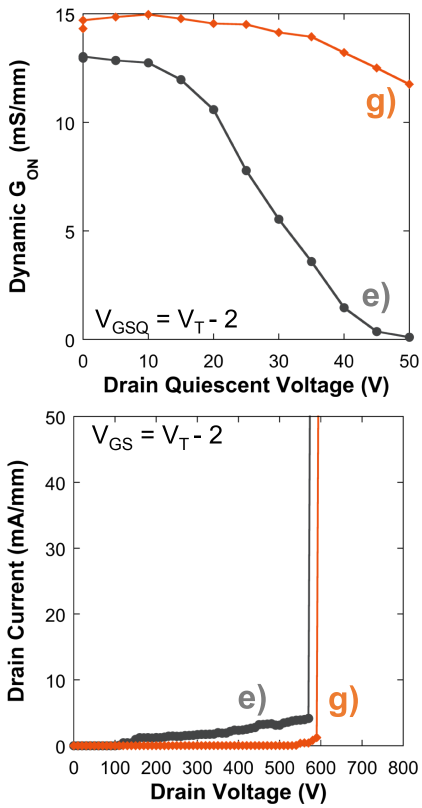

Fig. 5. a) Dynamic on-conductance and b) off-state breakdown characteristics of Samples e and g.

The impact of reducing the thickness of the annealed HF SiN is shown in Figures 6 and 7. Thinner HF SiN degrades the dynamic response, since the LF plasma during the mixed frequency step bombards the surface, creating damage. But, the thinner the annealed HF SiN is, the higher the breakdown voltage is.

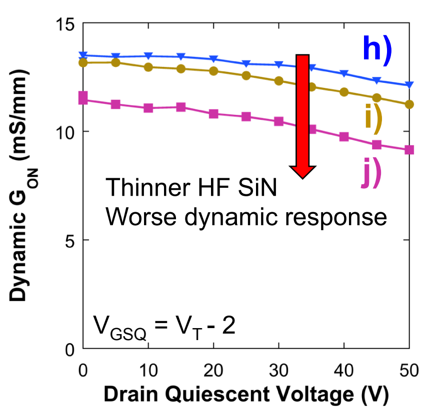

Fig. 6. Thinner annealed HF SiN degrades dynamic on-conductance with additional mixed frequency SiN on top.

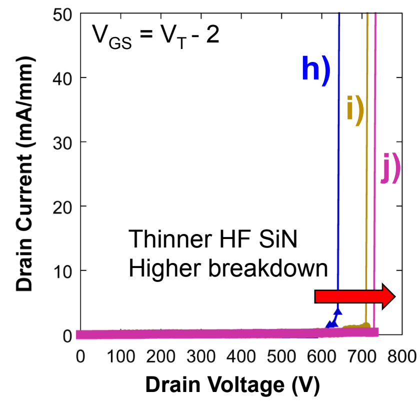

Fig. 7. Reduced thickness annealed HF SiN with additional mixed frequency SiN on top improves breakdown voltage.

Conclusions

The bi-layer SiN passivated GaN HEMTs result in poor off-state breakdown, the first approach is to densify and improve the quality of the HF SiN layer with a post-deposition 750 °C anneal for 30 minutes. Annealing the HF SiN resulted in a tradeoff between dynamic on-resistance and breakdown voltage. The unannealed HF SiN demonstrates good dynamic response, but poor breakdown, while annealed HF SiN has poor dynamic response, but good breakdown. Therefore, a modified bilayer SiN stack with 10 nm of annealed HF SiN and 100 nm of LF/HF SiN has improved breakdown and still has excellent dynamic response. Reducing the thickness of the annealed HF SiN reduces the negative threshold voltage shift imparted by the increased dielectric under the gate. However, reducing the annealed HF SiN from 10 nm to 3 nm degrades the dynamic response, but improves the breakdown voltage. Therefore, annealed HF SiN is one key parameter that can be engineered for the specific application.

Acknowledgements

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Acronyms

BOE: Buffered oxide etchant
HF: High frequency
HEMT: High electron mobility transistor
ICP: Inductively coupled plasma
LF: Low frequency
PECVD: Plasma enhanced chemical vapor deposition