Threshold Voltage Control by Tuning Charge in ZrO_2 Gate Dielectrics for Normally-off AlGaN/GaN MOS-HEMTs

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Abstract

Advanced applications of AlGaN/GaN high electron mobility transistors (HEMTs) in high power RF and power switching are driving the need for insulated gate technology. Here we present a MOS gate structure using ALD-deposited ZrO_2 as a high-k, high breakdown gate dielectric for reduced gate leakage, a recessed barrier structure for enhancement mode operation, and integrated passivation layers for reduced current collapse. Varying the precursor used for the gate dielectric, the amount of oxide charge can be controlled. This effect, combined with the optional gate recess, is taken advantage of the modulate the threshold voltage over a large range (7V).

INTRODUCTION

GaN-based high electron mobility transistors (HEMTs) are of significant interest for next-generation RF power amplifiers and monolithic microwave integrated circuits (MMICs). The integration of a gate dielectric in a MOS-HEMT device has been shown to offer significantly reduced gate leakage, resulting in improved reliability and reduced off-state power consumption. ZrO_2 has attracted increasing attention as a candidate gate insulator for GaN-based HEMTs, due to a high dielectric constant (25), large bandgap (5.9 eV), and high breakdown voltage (15-20 MV/cm). We have previously reported high positive threshold voltage in unpassivated HEMT structures with recessed barrier layers and ZrO_2 gate dielectrics deposited using zirconium (IV) tert-butoxide (ZTB) as the Zr precursor [1]. In this work, we compare these devices to structures incorporating the more common tetrakis(dimethylamino)zirconium (TDMA-Zr) precursor, which is expected to exhibit less fixed oxide charge. Combined with the optional barrier recess step, we demonstrate threshold voltage control over a range of 7V for a given HEMT layer structure. We also report the integration of SiN_X passivation layers and an evaluation of the dynamic switching performance of the devices.

RESULTS & DISCUSSION

AlGaN/GaN HEMT devices structures were grown on Si substrates by metal organic chemical vapor deposition (MOCVD). Devices were fabricated starting with a mesa etch in a Cl_2/Ar inductively coupled plasma (ICP) etch, followed by lift-off and rapid thermal annealing of a Ti/Al/Ni/Au ohmic stack and lift-off of Ti/Au overlay metal. An optimized bilayer SiN_X stack was deposited by plasma enhanced chemical vapor deposition (PECVD) [2]. A contact window and gate recess was etched through the SiN_X using SF_6 reactive ion etching (RIE), and a barrier recess was etched on some devices using a BCl_3/Cl_2/Ar ICP etch. The barrier recess was targeted to be a depth of 20nm, which is completely through the barrier layer. ZrO_2 layers (40nm) were deposited by atomic layer deposition using both ZTB and TDMA-Zr precursors and deionized water. Ellipsometry and X-ray photoelectron spectroscopy (XPS) were used to verify thickness (~40nm) and identify film stoichiometry. The gate metal was e-beam deposited Ni/Au. A cross section of the device structure is shown in Figure 1.

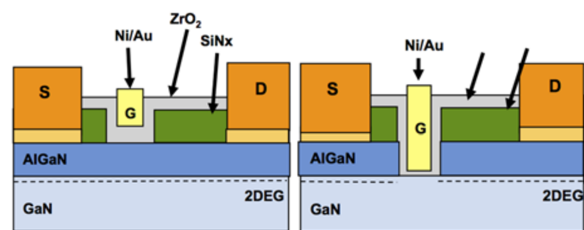

Fig. 1. Schematic of non-recessed (left) and recessed gate (right) MOS-HEMTs.

Capacitance-voltage measurements were initially used to characterize the oxide. A dielectric constant of 25 was extracted, and interface trap density was on the order of $\sim 1x10^{12}$, dependent upon the nature of the oxide and the surface upon which it was deposited (HEMT structure vs GaN MOS capacitor). Gated Hall measurements were used to characterize the 2DEG mobility and sheet carrier density, both in the HEMT structure and in the recessed region under the gate. The as-fabricated reference device had a sheet

resistance of 572 Ω/☐, mobility of 1618 cm^2/V-s, and sheet carrier density of 6.74x10^{12} cm^{-2}. Following recess etching, the channel was effectively eliminated as the sheet resistance increased to 80 kΩ/☐. Gated Hall measurements under +8V forward bias indicated restoration of channel charge to near the original values, but mobility was reduced an order of magnitude due to both the loss of the 2DEG channel and plasma damage under the gate. This is the primary factor limiting ON-state current in recessed barrier devices.

The FET device characteristics are summarized in Table I and shown in Figures 1 and 2. The non-recessed devices exhibit comparable current density, transconductance, and ON-resistance. The threshold voltage is shifted positive for device structures incorporating the ZTB-derived ZrO_2 film, approaching enhancement mode even without the barrier recess and demonstrating an exceptionally high +4V with a barrier recess. The mechanism for this is proposed to be the presence of negative charge in the oxide film, potentially due to excess oxygen in the film. The presence of such charge was verified on GaN capacitor structures. In contrast, the TDMA-Zr-derived ZrO_2 films exhibit a negative V_T shift due to the thicker effective barrier, just reaching enhancement mode operation even with a full barrier recess.

TABLE I
SUMMARY OF DEVICE CHARACTERISTICS

	Reference	ZTB	ZTB Gate Recess	TDMA-Zr	TDMA-Zr Gate Recess
V_T (V)	-2.11	-0.264	+3.92	-3.15	+0.113
$I_{D,MAX}$ (A/mm)	0.565	0.592	0.198	0.551	0.285
$g_{m, MAX}$ (mS/mm)	122	150	53.9	112	39.7
R_{ON} (Ω-mm)	17.1	9.93	22.7	10.9	24.5
$\Delta R_{ON,DYN}$ (%)	27.5	412	511	21	1

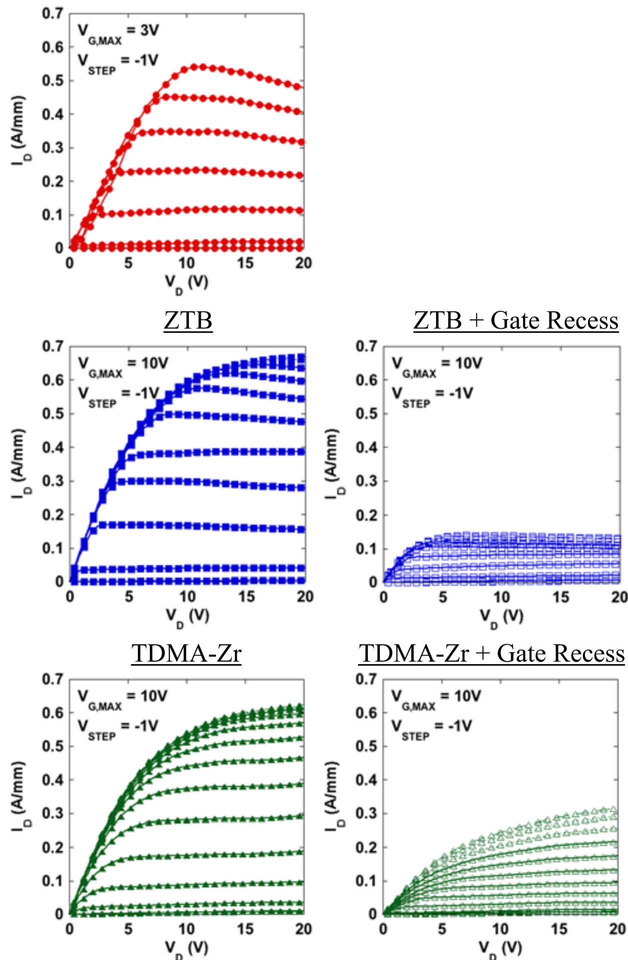

Fig. 2. I_D-V_D Characteristics of reference HEMT (top), ZTB-based MOSHEMT (middle), TDMA-Zr-based MOSHEMT (bottom).

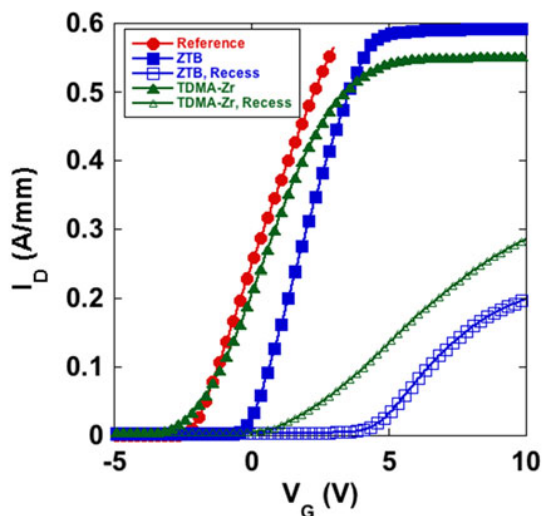

Fig. 3. I_D-V_G Characteristics of HEMTs.

As expected, the gate leakage was suppressed over 5 orders of magnitude compared to the reference Schottky gated HEMT, as shown in Figure 4. Pulsed I-V measurements (200ns) under OFF-state quiescent bias conditions ($V_{G,Q} = V_T - 2V$, $V_{D,Q} = 0$ to 50V) , shown in Figure 5 indicate a degraded current collapse behavior in the ZTB-based devices, which is expected as the negative charge from the oxide would be expected to enhance the charge trapping effect. In contrast, the TDMA-Zr-based device structures exhibit comparable current collapse to the reference device, and possibly even represent an improvement due to reduced trapping under the gate in the MOS structure. Similar behavior in the recessed gate structure indicates minimal permanent damage from the plasma recess etch. The breakdown voltage was comparable among all device structures both with and without recess, as shown in Figure 6.

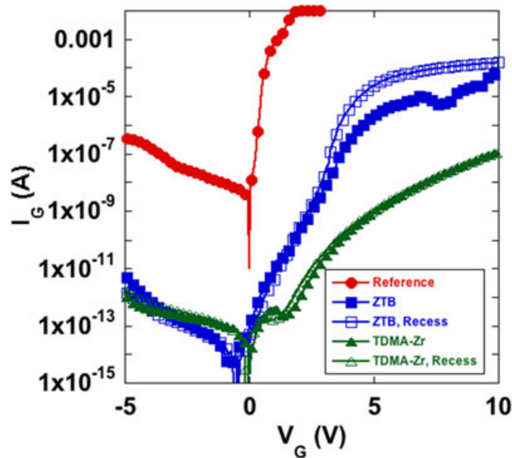

Fig. 4. Gate leakage behavior of MOS-HEMTs.

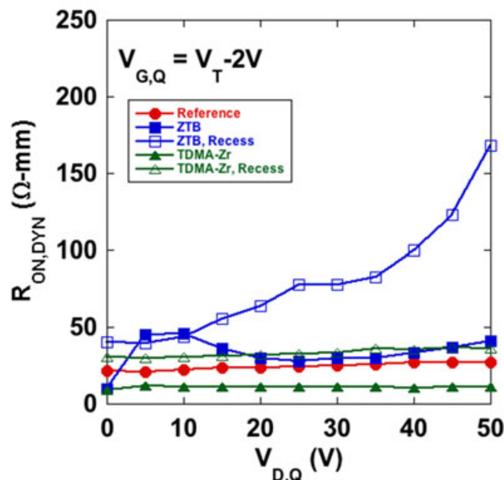

Fig. 5. Dynamic ON-resistance under OFF-state quiescent pulse conditions.

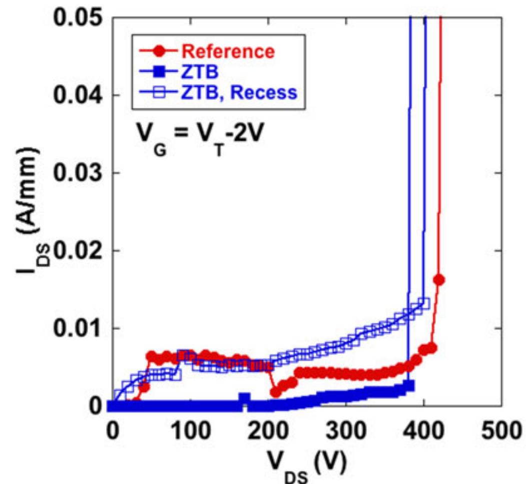

Fig. 6. Breakdown sweep for reference and ZTB-based MOSHEMTs.

Conclusions

In conclusion, we have demonstrated enhancement mode AlGaN/GaN MOS-HEMTs with a thin ALD-ZrO_2 gate oxide and barrier recess. The integration of this particular high-k dielectric in the device structure results in a positive threshold voltage shift when using the ZTB precursor due to negative charge in the oxide film and at the interface, which when integrated with a barrier recess enables a V_T ~+4V while suppressing gate leakage by 4 orders of magnitude compared to a reference Schottky-gated HEMT.

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References

[1] T.J. Anderson, V.D. Wheeler, D.I. Shahin, M.J. Tadjer, A.D. Koehler, K.D. Hobart, A. Christou, F.J. Kub, C.R. Eddy, Jr. "Enhancement Mode AlGaN/GaN MOS High Electron Mobility Transistors with ZrO_2 gate dielectric deposited by atomic layer deposition" *Appl. Phys. Express* 9, 071003 (2016)

[2] M.J. Tadjer, A.D. Koehler, C.R. Eddy, Jr., T.J. Anderson, K.D. Hobart, F.J. Kub. "Optimization of AlGaN/GaN HEMT SiN Passivaiton by Mixed Frequency PECVD" 2016 International Conference on Compound Semiconductor Manufacturing Technology, 307-309 (2016)