Design and Fabrication of High-Speed PIN Photodiodes for 50 Gb/s Optical Fiber Links

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Abstract

GaAs PIN photodiodes have been designed to act as receivers in 50 Gb/s optical fiber links, taking into account the fundamental delay components in a PIN photodiode. The devices were fabricated using a dry etching process and have gone through initial testing of dark current measurement and microwave modeling.

INTRODUCTION

The increasing demand for high-speed optical fiber links in data centers and high-performance computers drives the development of high-speed optical communication networks. Optical links based on energy-efficient directly modulated 850 nm oxide-confined VCSELs over multimode optical fiber are widely deployed. Recently, a direct-modulated VCSEL achieved record error-free data transmission of 57 Gb/s at room temperature [1] and 50 Gb/s at 85°C [2]. To complement such high-speed transmitters, high-speed receiver devices need to be designed properly so as not to present a bottleneck in the optical link. Currently, the most commonly deployed receiver in optical links up to 25 Gb/s is the traditional PIN photodiode based on GaAs or InGaAs. In this work, the design considerations and fabrication process of a high-speed GaAs PIN photodiode are described.

DESIGN

A typical PIN photodiode is operated in reverse bias, creating a constant electric field in the intrinsic region which acts as a light absorption layer. When light is shined on the photodiode, carriers are optically generated in the intrinsic region and swept towards the contacts by the electric field, generating a photocurrent. There are two main limiting factors to the high-speed operation of the photodiode: RC charging delay and transit time. The RC-limited bandwidth of a PIN photodiode can be expressed as follows:

$$f_{-3dB,RC} = \frac{1}{2\pi(R_S + R_L)(C_P + C_j)}$$

Where R_S is the series resistance of the photodiode, R_L is the load resistance, C_P is the parasitic pad capacitance, and $C_j = \frac{\epsilon A}{T}$ is the junction capacitance of the photodiode with area A and intrinsic region thickness T. The transit time is defined as the delay before an optically generated carrier is collected at the contacts and forms the photocurrent. The transit-limited bandwidth of a photodiode was calculated by Lucovsky et. al. [3]:

$$f_{-3dB,transit} = \frac{0.45T}{v_{sat}}$$

Where T is the intrinsic region thickness and is v_{sat} is the average saturation velocity of carriers.

From the two delay components, it can be concluded that the critical parameter for high-speed PIN photodiode design is the thickness of the intrinsic region. Following the method in [4, 5], the two bandwidths can be combined into a total bandwidth and plotted against the device dimensions to create design curves as shown in Fig. 1:

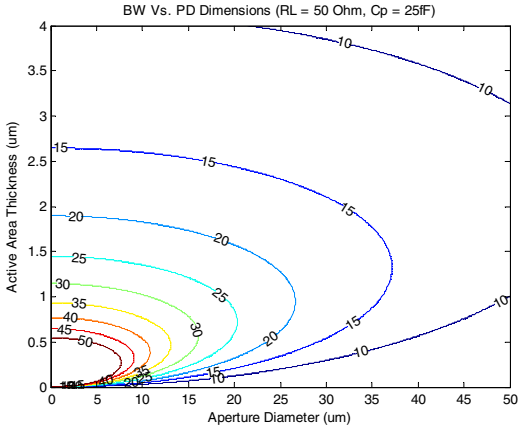

Fig. 1 (Color online). Design curves showing the bandwidth of the PIN photodiode as a function of intrinsic region thickness and aperture diameter A combined load resistance of 50 Ω and a parasitic capacitance of 25 fF were assumed.

For 50 Gb/s operation, f_{-3dB} of approximately 25 GHz is required. Following the design curves, the optimum photodiode dimensions are $T = 0.75\ \mu m$ and aperture diameter $R = 20\ \mu m$.

FABRICATION

For ease of fabrication and compatibility with high-speed VCSELs via optical fiber, a surface-illuminated vertical PIN photodiode structure with a circular aperture was chosen. A 0.75 µm GaAs intrinsic layer was selected to maximize responsivity. To prevent significant absorption in the p-region, an $Al_{0.2}Ga_{0.8}As$ optical window was used as the p-contact layer. With this configuration, the photodiode operates between 700 – 870 nm.

The fabrication process for the PIN photodiode is similar to the VCSEL fabrication process [1, 2]. After deposition of Ti/Pt/Au p-metal contacts to define the optical aperture, the photodiode mesa is defined using ICP-RIE with BCl_3/Ar plasma. Dry etching was preferred over wet etching in order to obtain straight sidewalls with minimum device capacitance. Afterwards, AuGe/Ni/Au contacts were deposited on an n-type GaAs contact layer with subsequent annealing at 310°C. A scanning electron micrograph of the device before planarization is shown in Fig. 2.

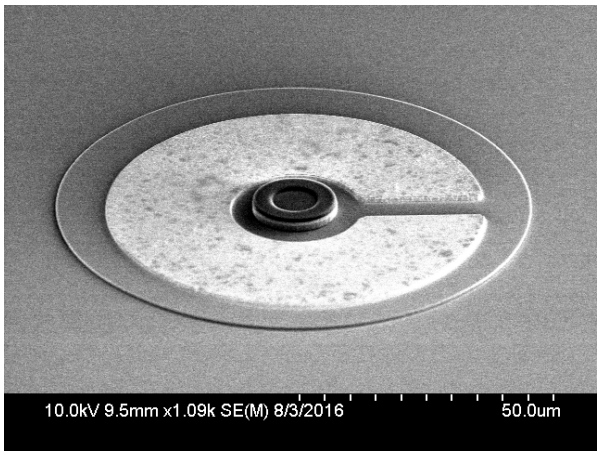

Fig. 2. PIN photodiode before planarization using BCB.

To passivate the device and to further reduce parasitic capacitance, the photodiode is planarized using BCB. A via is opened over the n-contact metal using CF_4 RIE before the top contact metal is deposited. Fig. 3 shows the final device after planarization, via opening, and top metal deposition.

CHARACTERIZATION & INITIAL RESULTS

The fabricated devices have gone through initial characterization consisting of dark current measurement and microwave modeling. The dark I-V curves of the PIN photodiode is shown in Fig. 4.

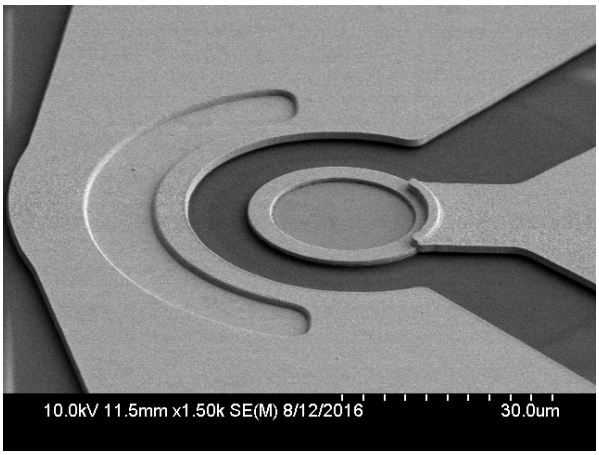

Fig. 3. Completed PIN photodiode after planarization, via opening, and top metal deposition.

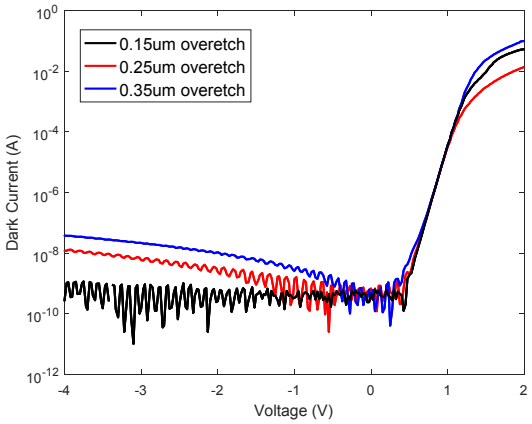

Fig. 4. Dark current of 20 µm aperture PIN photodiodes with various mesa overetch depths.

It was found that the dark currents vary based on the amount of unintentional overetch of the n-type GaAs contact layer during ICP-RIE etch. At reverse bias of -4 V, the dark currents are 1.1 nA, 12 nA, and 37 nA for 0.15 µm, for 0.25 µm, for 0.35 µm overetch depths, respectively. It is suspected plasma-induced damage on the vertical sidewall of the photodiode intrinsic region contributed heavily to the increase in dark current. Therefore, a minimal overetch is desired in the mesa etch process.

To extract junction and parasitic capacitances, a microwave model is constructed in Fig. 5 [6]. One-port s-parameter measurements are taken using a Keysight PNA using off-wafer calibration standards and on-wafer short-open de-embedding. The model is simulated using Keysight ADS and model parameters are adjusted to fit the measured s-parameters. The small signal model parameters are shown in Fig. 7.

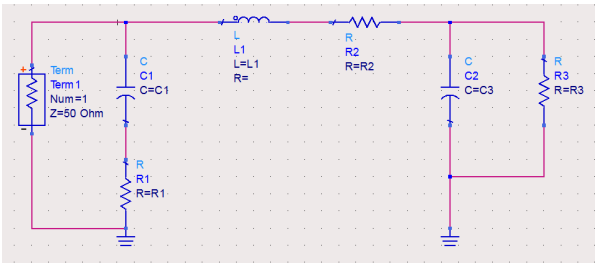

Fig. 5. Small-signal model of a PIN photodiode.

TABLE 1.
FITTED SMALL-SIGNAL MODEL PARAMETERS OF PIN PHOTODIODES WITH VARIOUS MESA DIAMETERS.

Diameter (um)	C1 (fF)	C3 (fF)	L1 (pH)	R1 (Ω)	R2 (Ω)	R3 (kΩ)
10	67.65	89.97	32.84	472.94	4.51	5.08
15	67.81	117.94	35.69	475.15	3.93	5.28
20	69.53	152.71	30.30	477.81	3.61	6.18
25	71.46	195.72	34.35	479.78	3.64	7.50
30	72.66	245.23	34.32	490.59	3.66	9.72
35	71.46	296.85	41.56	519.59	3.68	15.20
40	72.38	360.87	39.19	539.69	3.73	23.81

In particular, we are interested in the capacitor C3 which represents the photodiode junction capacitance. A plot of C3 against the junction area shows a linear dependence, as expected from a photodiode.

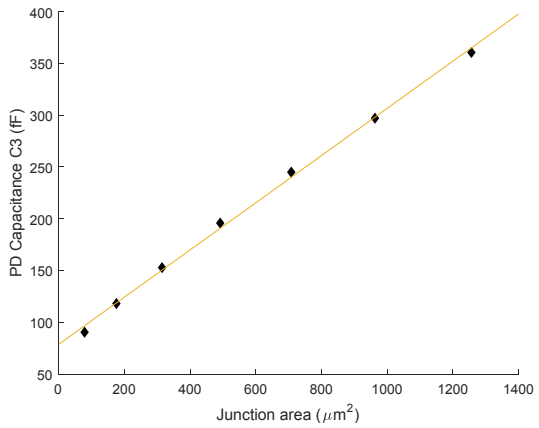

Fig. 6. Photodiode junction capacitance vs. aperture area.

CONCLUSIONS

GaAs PIN photodiodes have been designed and fabricated to operate as optical links up to 50 Gb/s. The photodiodes show dark currents of 1 nA. A microwave model has been used to extract the internal photodiode characteristics. At the time of writing, responsivity and bandwidths measurements are still underway.

ACKNOWLEDGEMENTS

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ACRONYMS

VCSEL: Vertical Cavity Surface Emission Laser
ICP: Inductively Coupled Plasma
RIE: Reactive Ion Etching