Comparison of Ion-Milling and Ion-Sputtering to Remove Edge Roughness of EBL Defined Emitter Metallization in InP/GaAsSb DHBTs

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Abstract

We compare two methods and their application to reduce the lithographically defined edge roughness of a Ti/Pt/Au HBT emitter metal stack: ion-milling with the Ionfab300 tool (Oxford) and ion-sputtering with Plassys-II. Reduction of the emitter metal edge roughness is desirable in order to decrease the base access distance between the emitter mesa foot and the self-aligned base metal, to effectively reduce the base resistance R_B and increase the maximum oscillation frequency f_{MAX}. Our work demonstrates that physical ion-bombardment of the emitter metal by both ion-milling and ion-sputtering prior to the emitter mesa dry etching indeed increases the maximal oscillation frequency f_{MAX}. However, ion milling significantly degrades device yield in comparison to the control and ion-sputtering processes. Ion-milling uses a charges neutralizer (Ionfab300) which may result in a more damaging ion bombardment.

Introduction

Type-II InP/GaAsSb double heterojunction bipolar transistors (DHBTs) show an excellent combination of bandwidth and breakdown voltages [1,2]. Recent results show InP/GaAsSb DHBTs reaching f_T/f_{MAX} up to 503/780GHz simultaneously [3]. Previous work [4] on HBT has shown an inverse dependence of f_{MAX} on the square root of effective time constant$(R_B C_{BC})_{eff}$. Therefore, a low base resistance R_B is necessary to achieve a high f_{MAX}. In this work, the process used to fabricate DHBTs features a self-aligned base metallization wherein emitter electrode is used as a mask for patterning base metal. As a result, the existence of emitter metal edge roughness is transferred to the distance (base access distance W_{ac}) between the bottom of emitter mesa and base metal, and eventually results in higher base resistance.

In this work, two different approaches are presented to mitigate the edge roughness of emitter metal: ion-milling and ion-sputtering. Compared to DHBTs without physical ion-bombardment, devices with both ion-milling and ion-sputtering show significant increases in their average f_{MAX} from 559 to 602/666 GHz, respectively. However, in terms of fabrication yield, ion-milling appears to degrade fabrication yield drastically to only 17 %, while ion-sputtering process maintains a relatively high device yield of 80 %, similar to the control samples without any ion-bombardment.

Experimental Details

For all three different emitter dry etching processes compared in this work, the same epitaxial layers used were grown at ETH Zurich by metal-organic chemical vapor deposition (MOCVD) on 2 in. semi-insulating InP substrates, following the design described in [2].

DHBTs were fabricated by a standard triple mesa process with 0.3 μm wide emitter and 0.4 μm-wide base electrodes defined by electron beam lithography (EBL). The emitter and base electrodes consist of electron-beam evaporated Ti/Pt/Au and Pd/Ni/Pt/Au metal stacks, respectively. The emitter mesa was formed by a combination of dry and wet etching. Dry etching was used to vertically etch the GaInAs cap layer, while wet etching was to shape InP. Inductively Coupled Plasma (ICP)-Reactive Ion Etching (RIE) has been conventionally [1, 2] used as the dry etching approach, however was found to leave a prominent roughness at the edge of emitter metal, which was then projected to the access distance W_{ac} due to the self-aligned base metallization, as shown in the scanning electron microscopy (SEM) image of the focused ion beam (FIB) cross section of finalized DHBTs (Fig.2). The standard method defines our control sample with an untreated emitter metal, Sample A. Two ion-bombardment methods were applied to different samples prior to ICP etching to remove the edge roughness: 1) Sample B was treated by Ar-ion milling in an Oxford Ionfab300 tool with an acceleration voltage 250 V, plasma Argon flow 10 sccm, etching time 160 s; 2) Sample C underwent Ar-ion sputtering in a Plassys-II tool with acceleration voltage 250 V, plasma Argon flow 8 sccm and etching time 160 s. After dry etching, the remaining GaInAs emitter cap layer acts as a mask for InP wet etching and thus determines the width of emitter-base junction. The emitter side-wall and extrinsic base surface were passivated before the formation of base-collector mesa. After the realization of base-collector mesa with a combination of dry and wet etching, collector electrodes were defined by photolithography and electron-beam evaporation. Two cycles of GaInAs/InP wet etching were performed

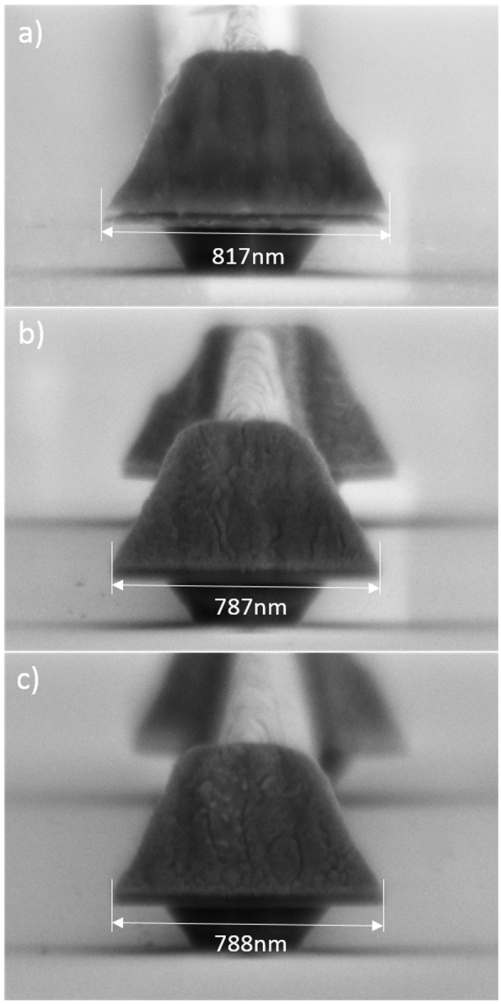

Fig. 1. SEM pictures of emitter mesa achieved with different dry etching approaches: a) Sample A: ICP-only; b) Sample B: Ion milling + ICP; c) Sample C: Ion-sputtering +ICP. The resulting emitter metal bone width are indicated by white arrows showing 817, 787, and 788 nm, respectively.

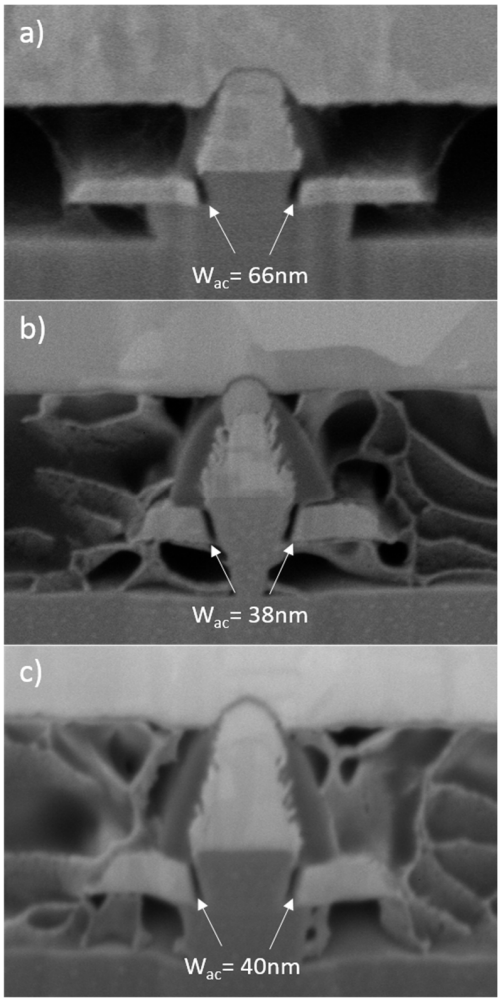

Fig. 2. SEM pictures of cross-sections of finished InP/GaAsSb DHBTs sliced by FIB. Devices were fabricated with different emitter dry etching processes: a) Sample A: ICP-only; b) Sample B: Ion milling + ICP; c) Sample C: Ion-sputtering +ICP. The base access distance shows 66, 38 and 40 nm, respectively. Damage to base and collector can be clearly observed in b).

afterwards to isolate transistors from each other, followed by a low-temperature (≤190 °C) Teflon-based etch-back planarization process [5]. Finally, the probe pad metal was deposited to enable future characterization.

Results and Discussion

Figure 1 shows the SEM images of half-completed devices on samples A, B, C, respectively, following emitter InP wet-etching. Samples B and C clearly exhibit smoother emitter metal edges, as well as a more vertical GaInAs sidewalls, which can be attributed to the physical ion-bombardment. The arrows in Figure 1 mark the actual emitter metal end widths

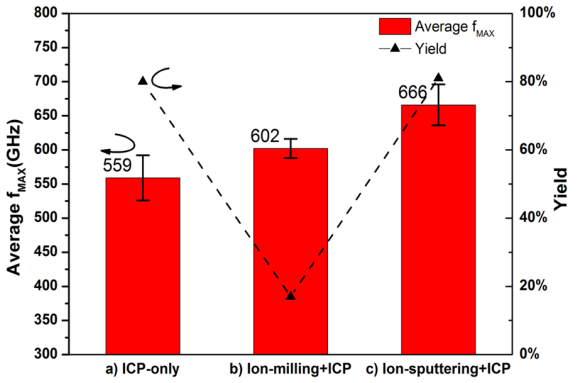

Fig. 3. Comparison of average maximal oscillation frequency f_{MAX} and yield of InP/GaAsSb DHBTs (W_E = 0.3 µm, L_E = 7.5 µm) fabricated with different emitter dry etching processes: a) Sample A: ICP only; b) Sample B: Ion milling + ICP; c) Sample C: Ion sputtering + ICP.

measured in each sample (design width =800 nm). The resulting widths of 787/788 nm in sample B /C compared to 817 nm in sample A confirm that ion-bombardment indeed reduced the emitter edge roughness, indicating a shorter base access distance can be expected after the subsequent self-aligned base metallization step. In order to inspect the real base access distances of DHBTs achieved in different samples, focused ion beam cross-sections were used to examine the intrinsic device regions, whose images were then captured by scanning electron microscopy (SEM) and displayed in Fig. 2. The white arrows in Fig. 2 indicate the actual base access distance W_{ac}. Compared to the original 66 nm in conventional ICP-only process, both ion-milling (38 nm) and ion-sputtering (40 nm) pre-treatment reveal significant reduction of W_{ac}. However, clear damage to the base and collector regions can be observed in the sample B treated with ion-milling. This damage explains the low yield found for sample B (See Fig. 3).

RF performance was characterized from 0.2 to 50 GHz with a PNA-X vector network analyzer calibrated with line-reflect-reflect-match (LRRM) techniques using off-wafer impedance standards. The probe pad parasitics were de-embedded iteratively taking advantage of the on-wafer OPEN and SHORT structures designed with the same layout as the device probe pads. Figure 3 summarizes the RF performance of 7.5-μm-long devices on different samples. The average maximal oscillation frequency (f_{MAX}) of functional devices shows 559±33, 602±14 and 666±30 GHz for Sample A, B, C, respectively. In the present context a device is deemed functional if its f_{MAX} exceeds 80% of F_{AVE} (626/664/708 GHz, the average f_{MAX} of top 10 fastest devices on each chip). From 35/35/27 measured devices from samples A/B/C, 28/6/22 devices were deemed functional, corresponding to a yield of 80/17/81 %, respectively. Judging from these numbers, ion-bombardment treatment, either ion-milling or ion-sputtering, prior to emitter ICP etching apparently improves the transistor RF performance, however, ion-milling delivers an extremely low yield, which is indicated by the partially damaged base and collector observed in Fig. 2b. One possible reason for this observed damage is the stronger and more continuous ion bombardment achieved by ion-milling. The Ionfab300 tool used in this work is equipped with a neutralizer to counteract the accumulated positive charges on the sample surface, enabling a stronger and continuous ion bombardment of the surface, whereas in the Plassys-II tool the accumulated positive charges stay at sample surface and weaken the energy of after-coming ions, resulting in a milder bombardment.

CONCLUSIONS

We demonstrated that ion-bombardment treatment (ion-milling/ion-sputtering) prior to emitter ICP dry etching removed the edge roughness of emitter metal stack, and reduced base access distance W_{ac} from 66 to 38/40 nm, leading to an improvement of average f_{MAX} from 559 to 602/666 GHz. However, ion-milling approach was found to harm the transistor base and collector, leaving an extremely low yield of 17 %, compared to 80 % for ICP-only control sample. In contrast, simple non-neutralized ion-sputtering method (with a yield of 81 %) does not reduce yield compared to control sample.

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ACRONYMS

DHBT: Double Heterojunction Bipolar Transistor
MOCVD: Metal-Organic Chemical Vapor Deposition
EBL: Electron Beam Lithography
ICP: Inductively Coupled Plasma
RIE: Reactive Ion Etching
SEM: Scanning Electron Microscopy
FIB: Focused Ion Beam